

# *Schematic and Layout Guidelines for PI6CV304/PI6CV2304*

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Today's high-speed requirements are challenging hardware designers to a new level. With current speeds, any flaw in a design can mean the difference between a working system, and a non-working system. With any design, having the proper layout is one of first and most important considerations. This application note will discuss some layout techniques to achieve the best performance when using Pericom's PI6CV304 and PI6CV2304 clocks.

## **PI6CV304/PI6CV2304**

Pericom's PI6CV304 and PI6CV2304 are low-skew, low-noise, high-speed clock buffers that are ideal for computing, networking, and communications applications. Application examples include PCI(X) clock buffers in servers and workstations, PCI(X) Storage Area Network (SAN), and RAID controllers. They can be used for networking and communication applications requiring 80MHz for 10/100 Mbs Ethernet, and 125 MHz for Gigabit networking clocks.

Pericom's PI6CV2304 integrates a 30-ohm resistors on all outputs

## **Decoupling Capacitor**

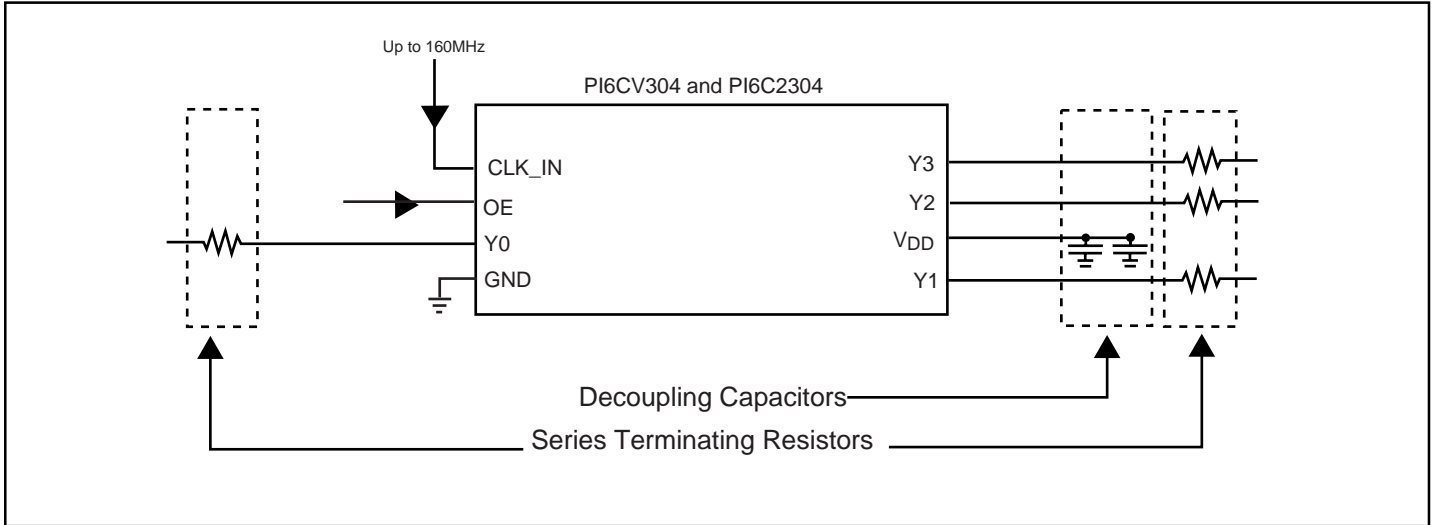
Decoupling capacitors are very critical in terms of limiting noise. Without proper decoupling capacitors to minimize heavy  $V_{DD}$  ripple and GND bounce, it can cause system-false triggering or may even cause complete system failure.

Noise on the  $V_{DD}$  line (ripples) and GND (GND bounce) can also drastically increase skew and output jitter. To minimize noise to the device's  $V_{DD}$  and GND, a high-frequency ceramic (surface mount recommended) 0.47 $\mu$ F and a 0.01 $\mu$ F bypass capacitor should be connected as close as possible between  $V_{DD}$  pin and GND pin. In addition to the 0.47 $\mu$ F and a 0.01 $\mu$ F, there should also be a sufficient amount of decoupling capacitors added to the main power supply. Figures 1 and 2 show the schematic and layout conditions for the PI6CV304.

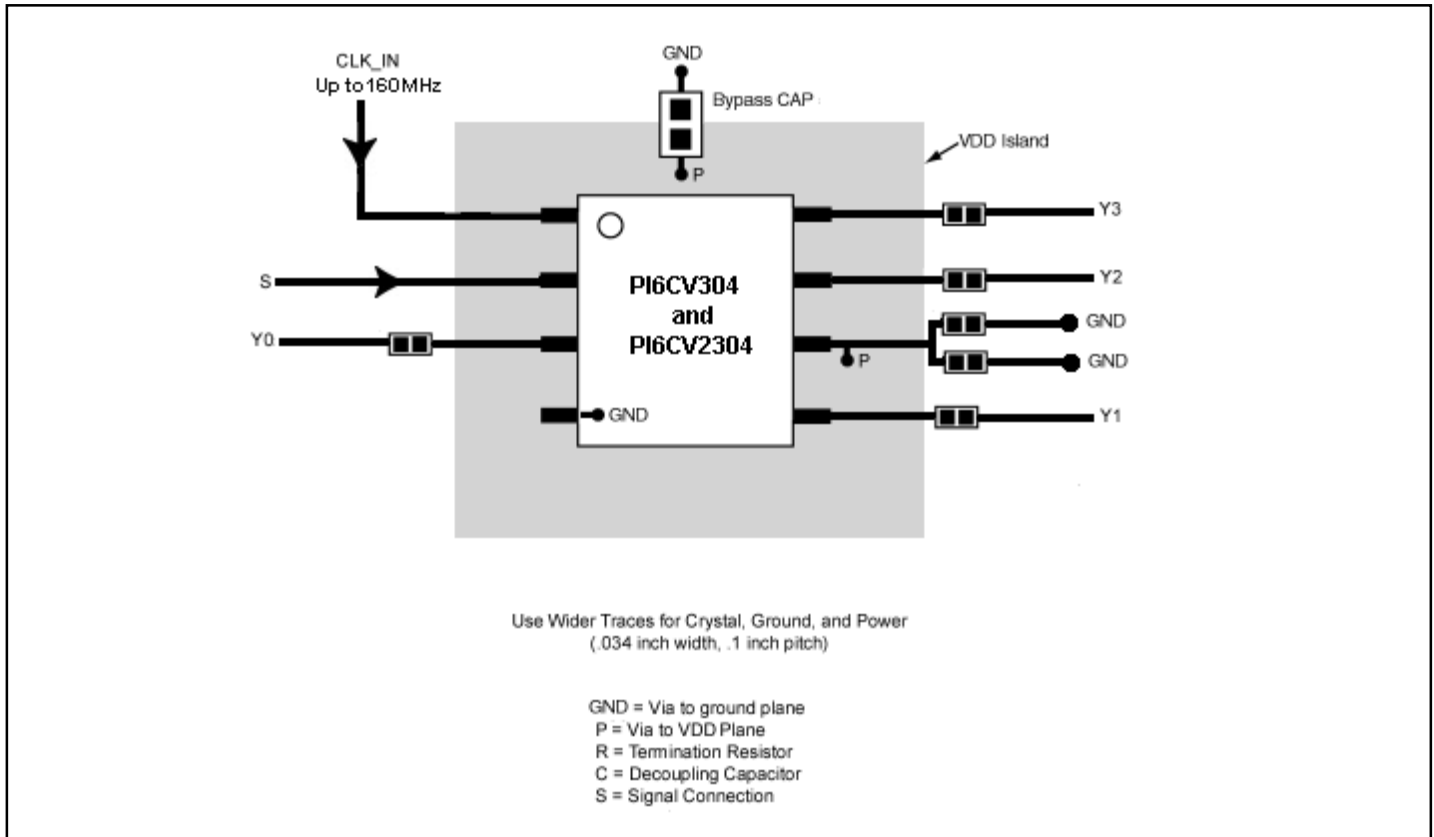
Here are some recommendations for the PI6CV304 and PI6CV2304. But it should be noted that the recommendations may vary from one application to another.

## **Recommendations**

1. A 0.47 $\mu$ F and a 0.01 $\mu$ F decoupling capacitors should be connected between the  $V_{DD}$  and GND for all  $V_{DD}$  pins. Placement of the decoupling capacitors should be connected as close as possible to the  $V_{DD}$  pin of the device (within 2mm recommended).
2. In addition to the 0.47 $\mu$ F and 0.01 $\mu$ F decoupling capacitors connected between  $V_{DD}$  and GND of the device, there should be a sufficient amount of capacitance added to the main power supply.
3. Output impedance is approximately 20-ohm for the PI6CV304 and approximately 33-ohm for the PI6CV2304. When using a termination resistor, it should always followed the following equation:  $R(\text{output impedance}) + R(\text{termination}) = R(\text{trace})$ .
4. Use a controlled impedance trace with proper termination to match the trace's impedance. Note that the PI6CV2304 has an internal 30ohm termination resistor for all of the outputs.
5. Minimized the trace length to be as short as possible.
6. Avoid looping the clock signal if possible. If serpentine technique is required to maintain equal trace length, use arcs or 45° turns rather than 90° turns thereby avoiding impedance discontinuities.
7. Use minimal vias to avoid impedance discontinuity (which introduces more skews and reflections).
8. Keep high-speed buses and logic away from the clock devices to prevent noise couple onto the clock signals.
9. Placement of the clock device should be at the center of all other components so that the clock signal traces are kept to a minimum.
10. Use a solid GND plane, and do not route any signal in the GND and power plane.



**Figure 1. Schematic for the PI6CV304 and PI6CV2304.**



**Figure 2. Layout for the PI6CV304 and PI6CV2304.**