

PI6C2502 Zero-Delay Clock Buffer

Layout and Schematic Guidelines

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Introduction

Because of today's high-speed design demands, board designers must have extensive knowledge concerning transmission line effect, EMI, and crosstalk. They also need to understand board materials, signal and power stacking, connectors, cables, vias, and trace dimensions. Pericom Semiconductor Corporation offers an extensive line of high-speed clock products for desktop, notebook, set top boxes, information device, servers, and workstations. To make high-speed chips function properly, a designer needs to rely on accurate schematics and layout guidelines.

This application note focuses on Pericom's PI6C2502 Zero-Delay Clock Buffer, presenting schematics and layout guidelines for the chip. Also listed are some decoupling guidelines that are important for this chip's varied applications.

Decoupling Capacitors

Every printed circuit board needs large bypass capacitors to balance the inductance of the power-supply wiring. These capacitors have some lead inductance that increase as the frequency goes higher, which is why it is very important to place the capacitors as close as possible to the *VCC and Ground Pins on the Chip*.

To reduce the series lead inductance effect, avoid the following:

1. Long traces larger than 0.01 inch between capacitor pad and via
2. Use of capacitors other than surface mount
3. Via holes less than 0.035-inch diameter

Pericom's clocks use high-precision, integrated analog PLL that can be effected by the power supply and ground pins. Noise on these two pins can dramatically increase skew and output jitter.

To minimize these problems, connect a 4.7µF, a 220nF, and a 2.2nF capacitor to the digital supply pin. Also use one 4.7µF, one 220nF, and one 2.2nF capacitor on the analog supply pin. Connect the other side to the analog ground pin.

Place a 10µF capacitor from the main power island to the power plane that is supplied to the clock chip.

Use high-quality, low ESR, ceramic surface-mount capacitors.

Stacking

At low speeds, currents follow the least resistance path, but at high speeds current follows the least inductance path. The lowest inductance return path lies directly under the signal conductor.

This location minimizes the total loops needed between the outgoing and returning paths. That is why it is important to separate the signal layers by ground planes if possible. Also avoid totally cutting part of the ground plane to be used for a signal's path. That is totally unacceptable, because it will increase crosstalk considerably and does not provide a clean return to those signals. Also use lower trace impedance because it lowers undershoot and overshoot. Always use FR-4 material for board fabrication. Use 4-layer stack-up arrangement. Make sure you have a signal layer that is followed by the ground layer, then a power layer, and finally the second signal layer. Please see Figure 1 below.

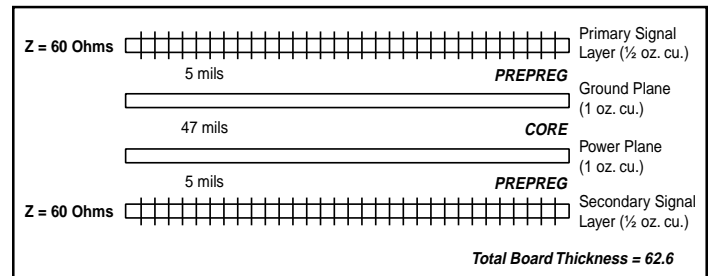


Figure 1: Four-Layer Board Stack-up

Clock routing and spacing

To minimize crosstalk on the clock signals, use a minimum of 0.014-inch spacing between clock traces and others. If you have to use serpentine to match trace lengths on similar chips, make sure that you have at least 0.018-inch spacing for serpentes. Please see Figure 2 below.

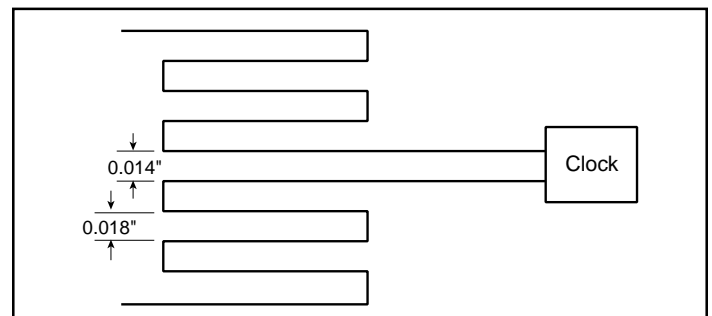
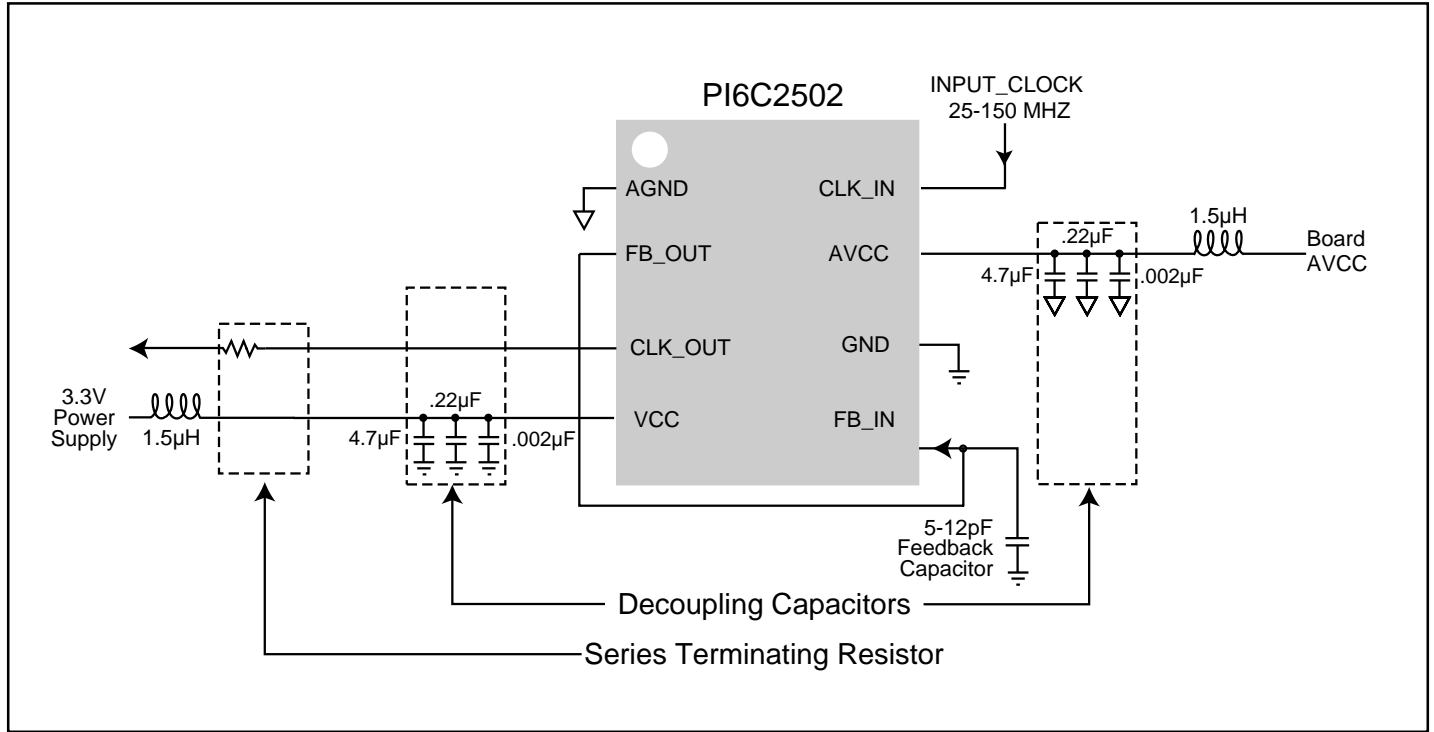


Figure 2: Clock Trace Spacing Guidelines

Schematic Drawing



Clock Chip Layout

