

PI6C2502 Performance in RAID Storage Applications

Introduction

The PI6C2502 is a 3.3V low-skew, low-jitter, phase-lock loop (PLL) clock driver. By connecting the feedback output to the feedback input the propagation delay from the CLK_IN input to the output will be nearly zero.

When used in conjunction with the Intel GC80303 (Zion) processor in a PCI application the system designer must determine the power and ground connections, stop-clock characteristics, and the reference clock input circuit. This application note will provide the designer with the necessary information to implement the PI6C2502 into an environment with a 33 MHz or 66 MHz reference clock input.

The 33 MHz PCI clock is typically 5V and the 66 MHz PCI clock is typically 3.3V. Although the PI6C2502 is not 5V tolerant, a series resistor on the reference clock input will allow interfacing to a 5V signal. The specifics of connecting the PI6C2502 to a 5V input are explained further in this application note.

Stop-clock Characteristics

During sudden power loss to the system the clock reference signal on CLK_IN may suddenly stop and stick HIGH or LOW. Once the input clock is no longer detected, the PI6C2502 output will continue to oscillate. This is due to the PLL phase detector cannot track the input due to the sudden change of frequency, i.e., from 33 MHz to 0 MHz instantaneously. The output will slow in frequency and eventually stop oscillating, however, these few extra cycles may be enough for a storage system to save valuable data to memory.

Two cases are examined in this application note, 66 MHz and 33 MHz reference input clock frequencies. For both cases the results are the same for the clock stopped either logic HIGH or LOW. The PLL was locked and running before the reference stopped. Figures 1 to 6 depict the PI6C2502 stop-clock characteristics.

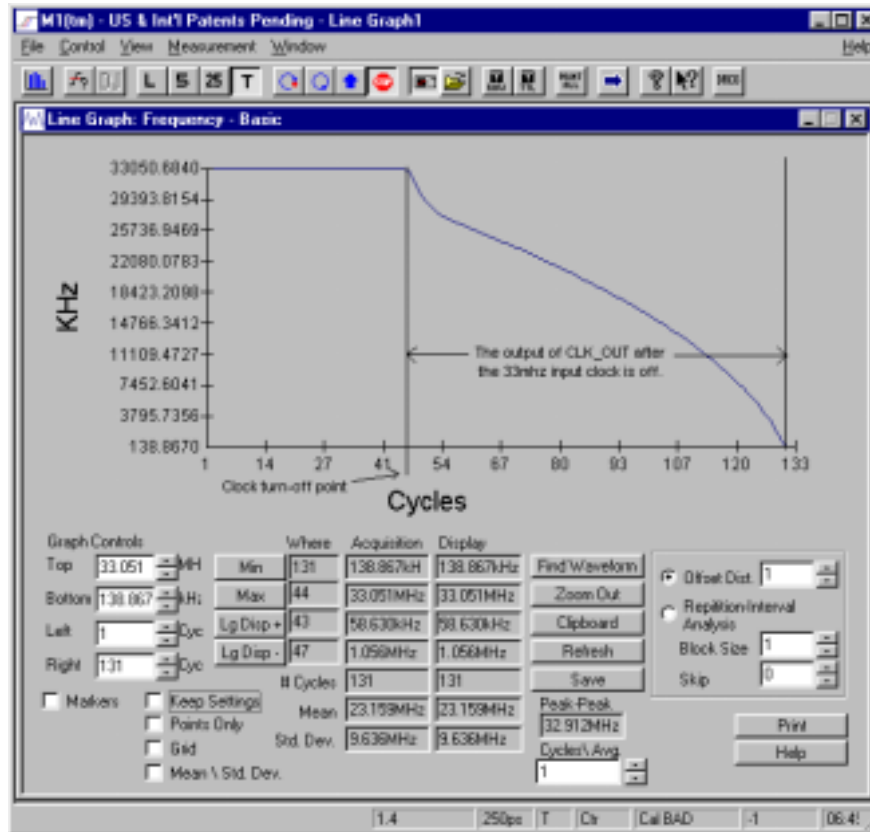


Figure 1. The PI6C2502 output at CLK_OUT before and after the 33 MHz input clock is turned off.

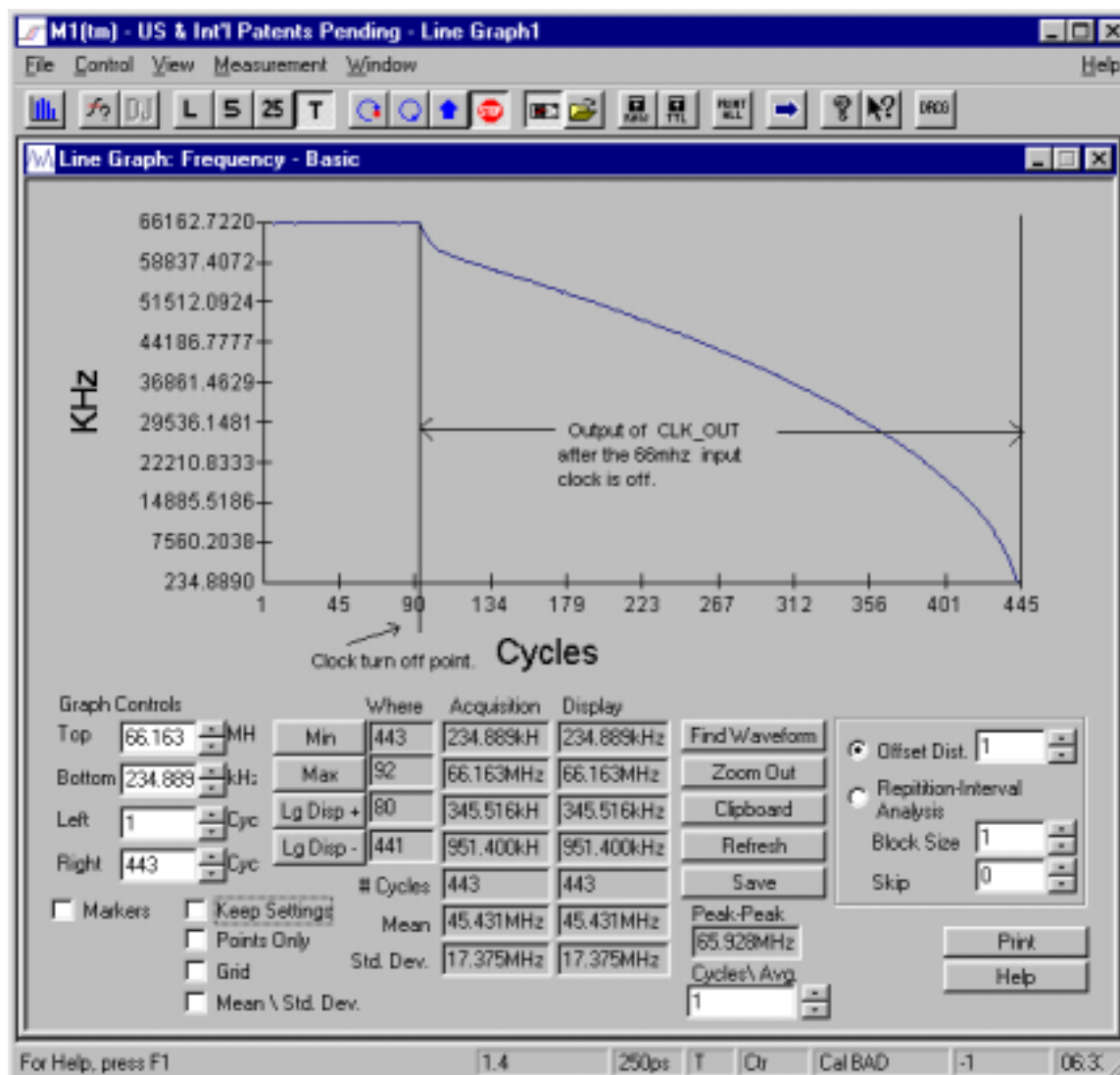


Figure 2. The PI6C2502 output at CLK_OUT before and after the 66 MHz input clock is turned off.

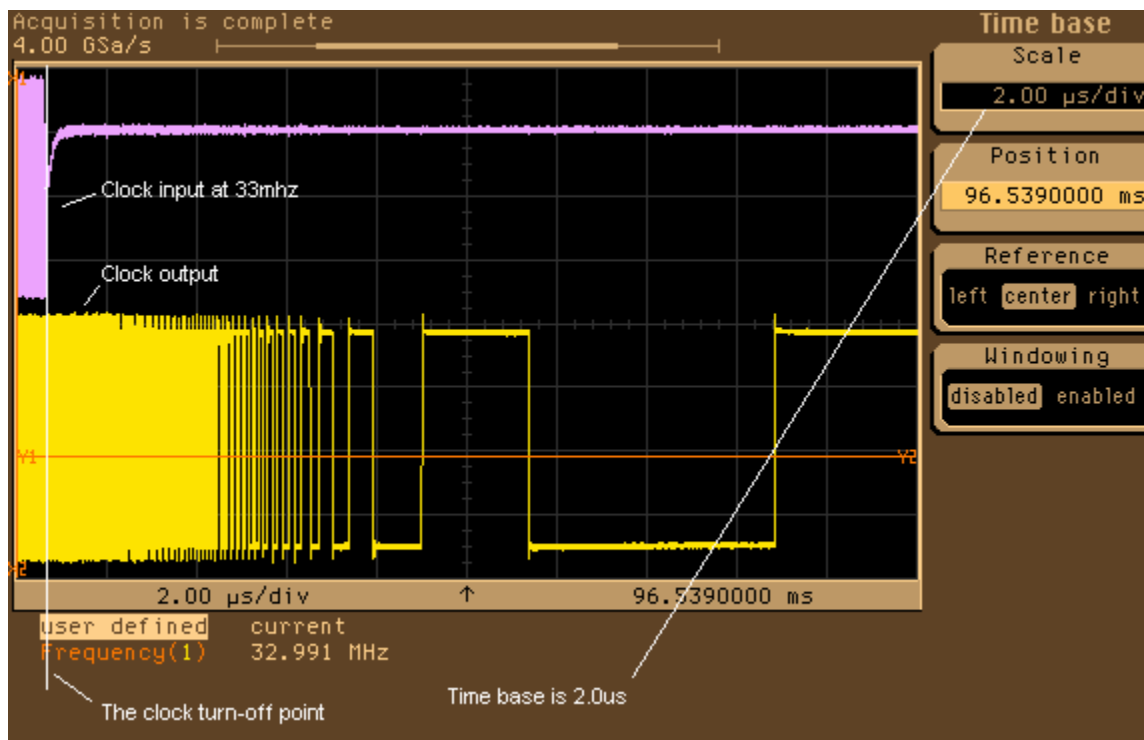


Figure 3. Input clock is 33 MHz. Measured at time base 2.0 μ s, clock input is ended with logic HIGH.

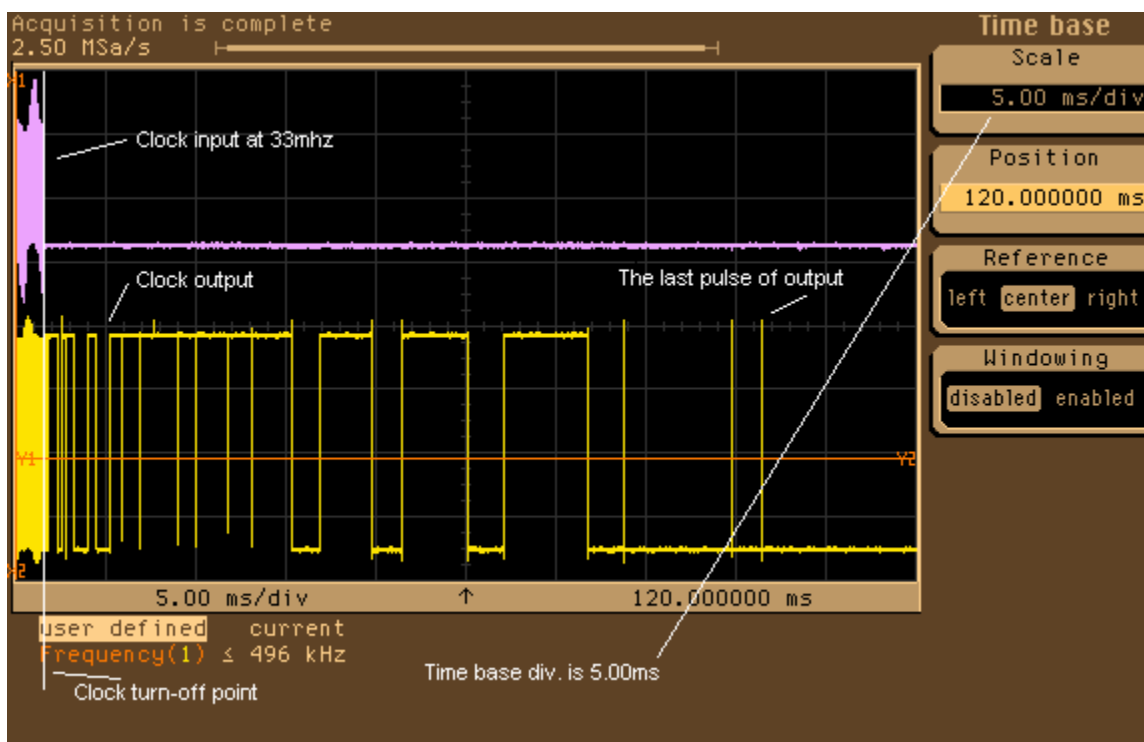


Figure 4. Input clock is 33 MHz. The test condition is the same with Figure 3, but measured at time base 5.0ms and clock input ended with logic LOW.

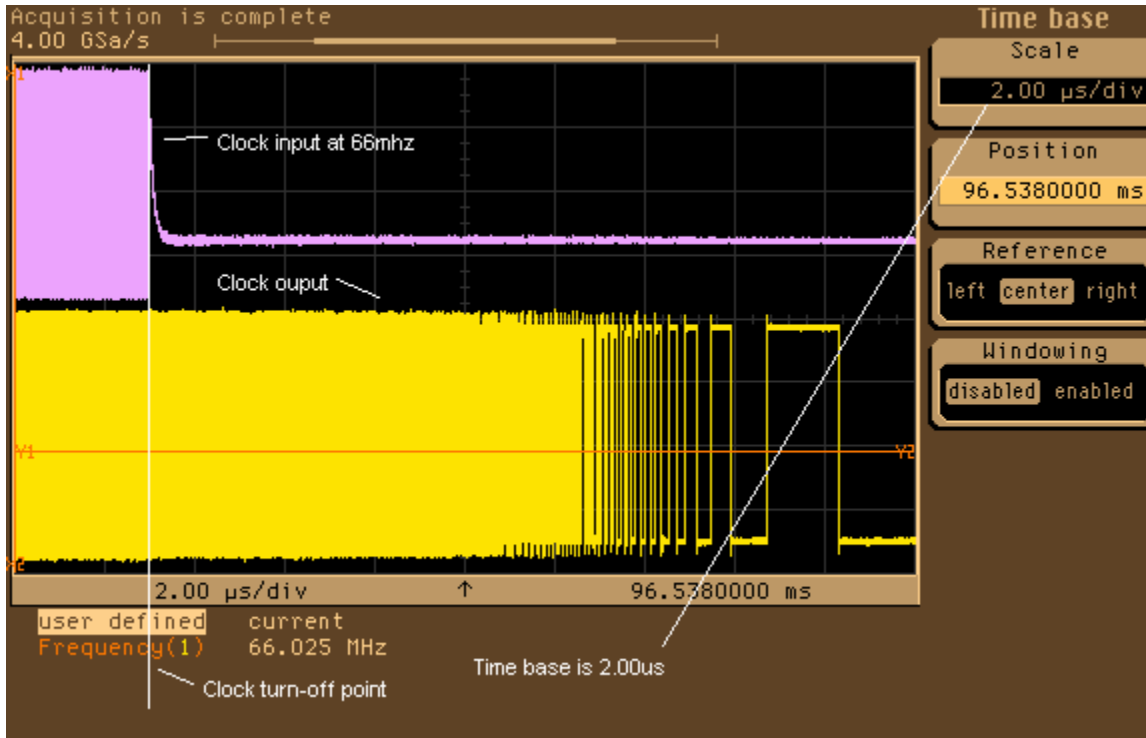


Figure 5. Input clock is 66 MHz. Measured at time base 2.0μs, clock input is ended at logic LOW.

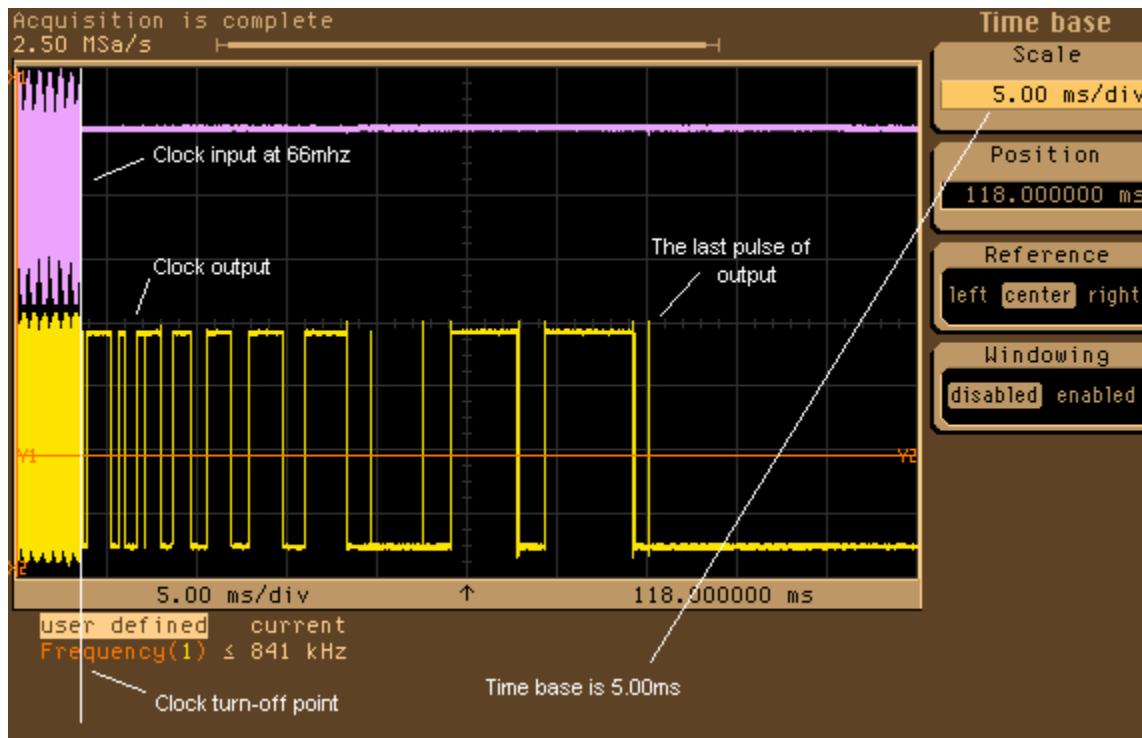


Figure 6. Input clock is 66 MHz. The test condition is the same with Figure 5, but measured at time base 5.0ms and the clock input ended with logic HIGH.

5V to 3.3V Clock Reference Input Circuit

The PI6C2502 is a 3.3V device and is not 5V input tolerant. Typically the 33 MHz interface 5V and the 66 MHz interface is 3.3V. If a 5V input is present on CLK_IN, then the internal clamping diode to V_{CC} will forward bias – **destroying the device**. Following is a solution for an input circuit that will protect the PI6C2502 when a 5V input clock is used on CLK_IN.

Figure 7 shows the PI6C2502 5V to 3.3V interface circuit. The purpose of R_{clk_in} is to limit the input current. R_{clk_in} is fixed at 330 ohm and the input current at CLK_IN is 2.76mA when input clock is 5.0V at 66 MHz, 33 MHz and DC. If R_{clk_in} is larger, then the input current will be smaller, but the RC time will be longer and the frequency of input clock will be limited. Conversely, if the R_{clk_in} is smaller, then current will be larger (See Figure 8 for the RC time delay on pin CLK_IN and pin FB_IN).

The PI6C2502 board was tested with a 330 ohm R_{clk_in} at input frequencies of 33 MHz, 66 MHz and up to 180 MHz. The output of PI6C2502 tracks well until 180 MHz and lost track at 183 MHz. Since there is a 1.2ns time delay between clock input (at point A) and clock output caused when R_{clk_in} is 330 ohm, it is necessary to add R_{fb_in} on pin FB_IN in series to compensate the time delay. When R_{clk_in} is 330 ohm and R_{fb_in} is 280 ohm, the time delay between CLK_OUT and CLK_IN (point A) is zero (see Figures 10 and 11) at clock 66 MHz and 33 MHz. If the value of R_{fb_in} from 470 ohm to 0 ohm is adjusted, then the time delay between CLK_OUT and CLK_IN (point A) will be changed from +1.2ns to -700ns (See Figures 8 and 9). The skew for 280 ohms will be 200ps leading skew for 5V and 200ps lagging skew for 3.3V.

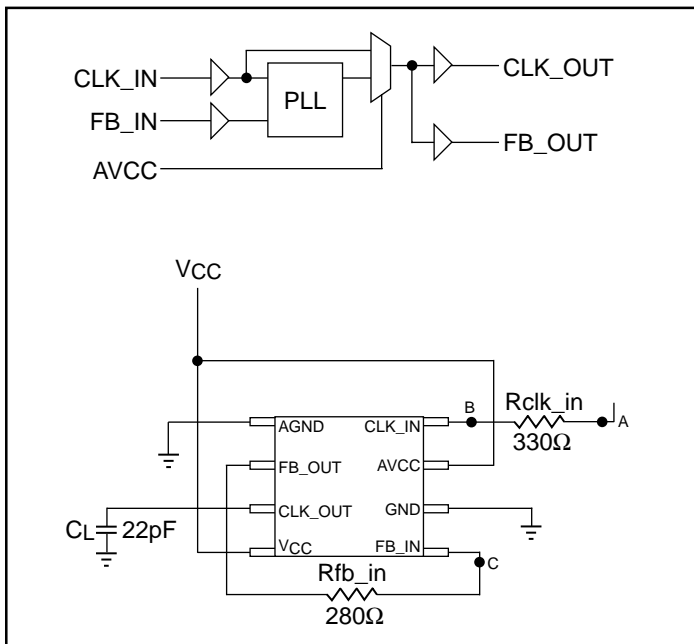


Figure 7. PI6C2502 block diagram & circuit of 5V to 3V interface solution.

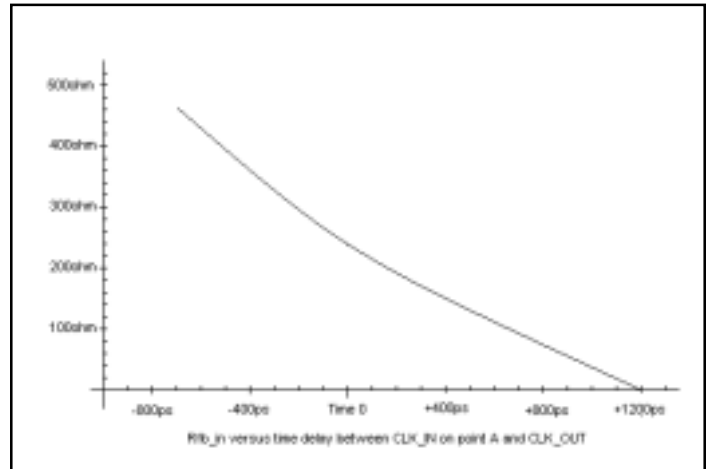


Figure 8. Time delay because of R_{fb_in}

R _{fb_in} value (R _{clk_in} = 325.6ohm)	Delay between clock output and input
464.4ohm	-700ps
325ohm	-400ps
239ohm	Zero delay
217ohm	+200ps
109ohm	+550ps
0ohm	+1.2ns

Figure 9. Zero delay between CLK_OUT and CLK_IN at 66MHz.

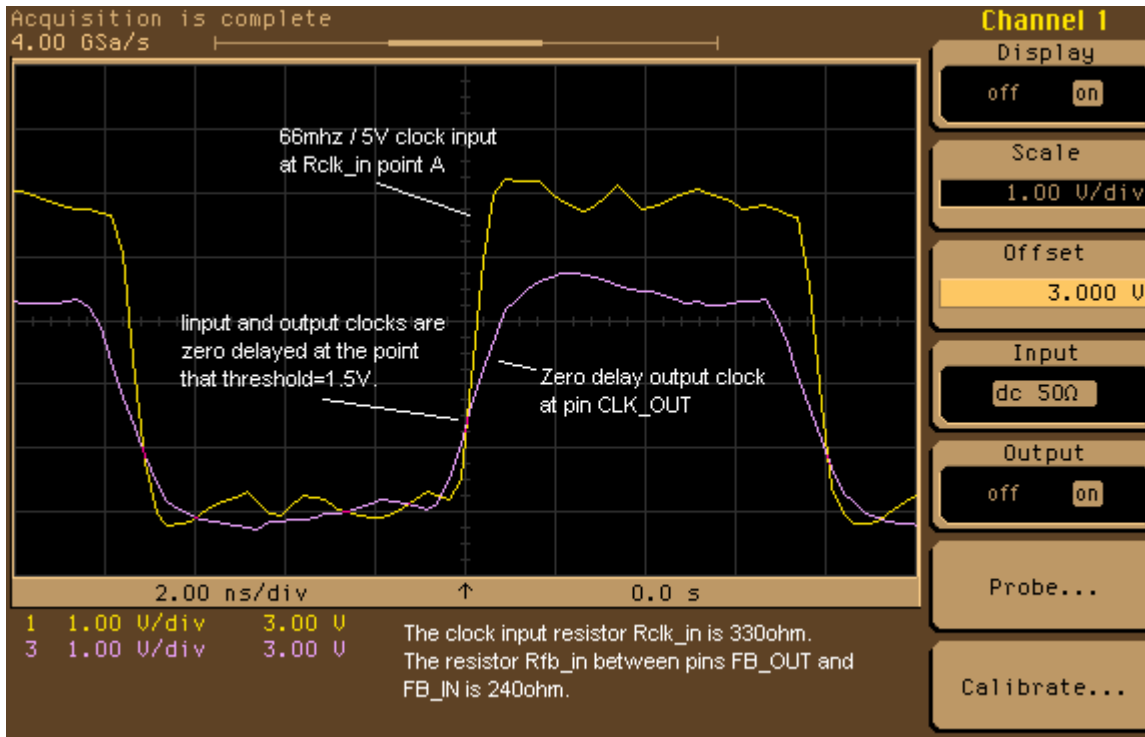


Figure 10. Zero-delay between CLK_OUT and CLK_IN at 66 MHz.

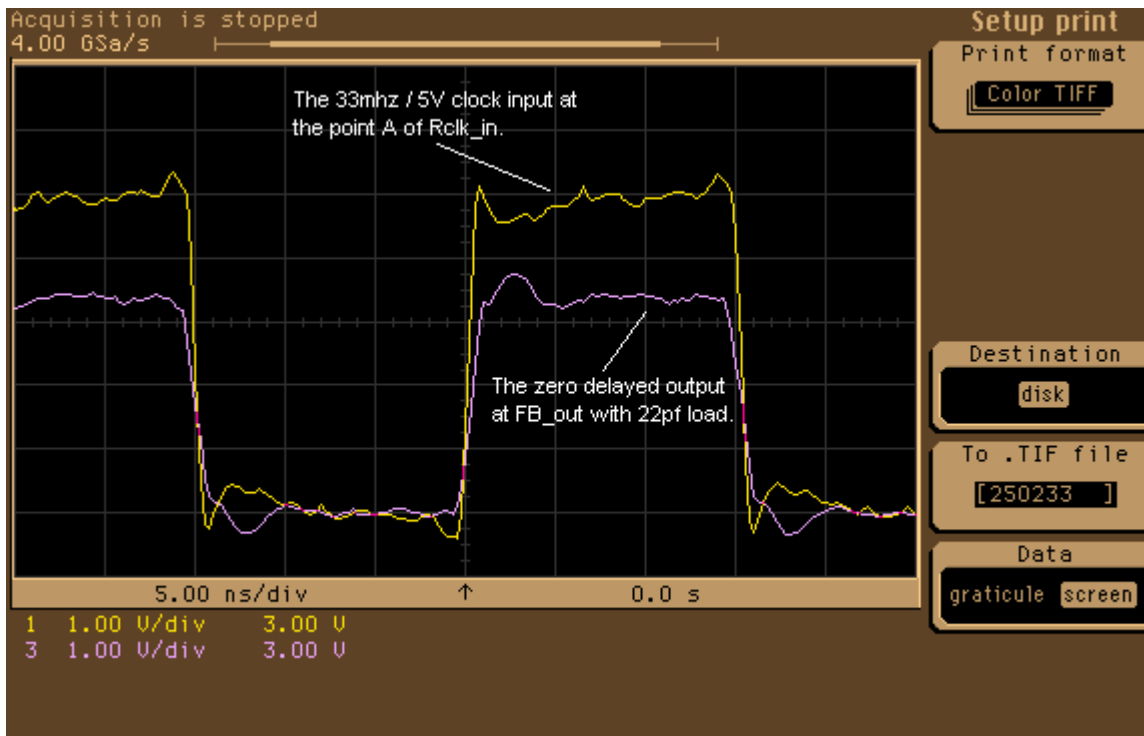


Figure 11. Zero-delay between CLK_OUT and CLK_IN at 33 MHz.

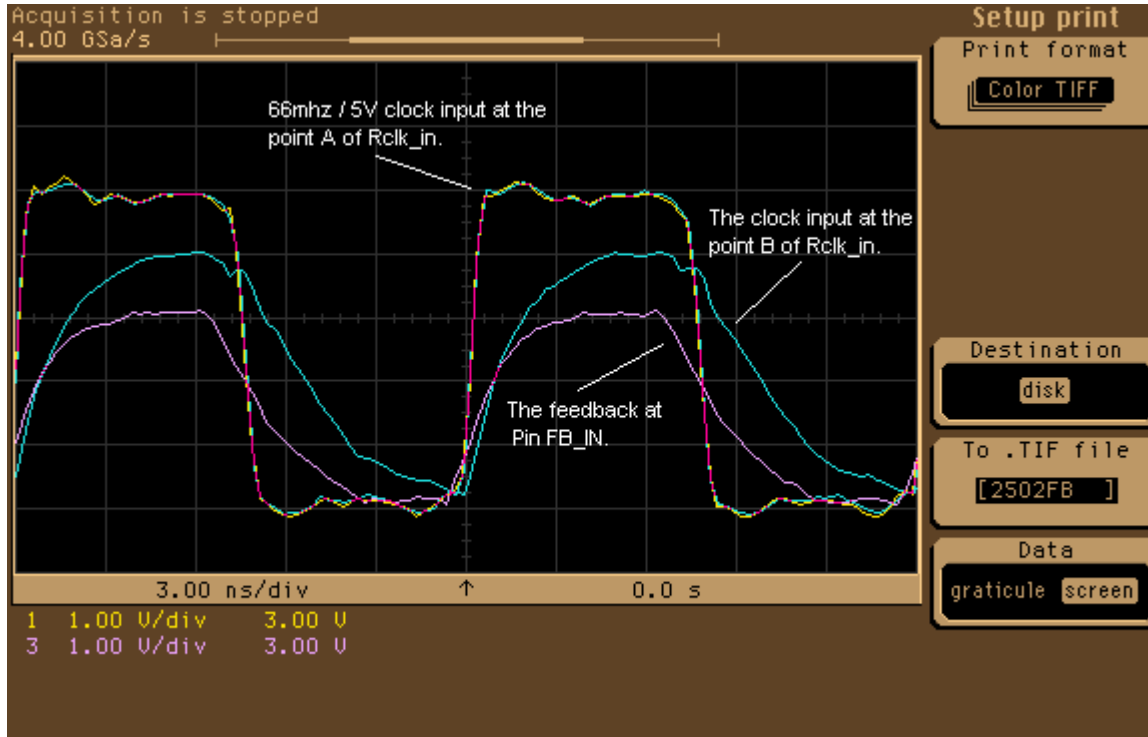
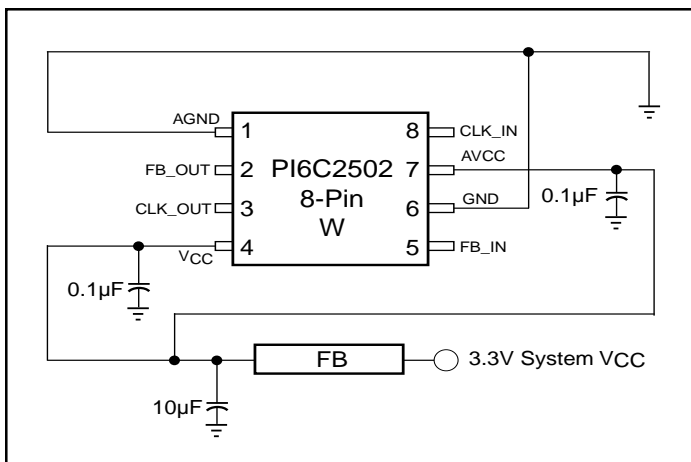


Figure 12. RC time delay on pin CLK_IN and pin FB_IN.

Power and Ground Connection

Connect AGND and GND to the common system ground plane. Use a ferrite bead on the 3.3V System V_{CC} to block high frequency noise from the power supply. Place a 10 μ F capacitor as close to the ferrite bead as possible to eliminate low frequency noise from the power supply. A 0.1 μ F capacitor to ground should be placed as close as possible to the device V_{CC} and AV_{CC}.



Summary

The PI6C2502 can be implemented in a storage application to guarantee a valid clock output even when the reference clock is stopped. These additional clock cycles can be used to clock a memory interface so vital data can be moved into memory. The actual number of cycles will vary, depending if the input clock is 66 MHz or 33 MHz.

A series resistor must be placed on the PI6C2502 input if a 5V reference clock is used. Included in this application note is the suggested interface circuit for the PI6C2502 to a 5V input. Refer to the PI6C2502 datasheet for the device specifications.