

PI6C2510-133 Performance in Registered PC133 SDRAM DIMM Modules

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Pericom Semiconductor offers nine and ten output, zero-delay buffers that meet and exceed the IBM PC133 specification revision 1.1. This application note outlines the performance of Pericom’s PI6C2510-133 in a planar PC133 SDRAM Registered DIMM module. Addressed are critical parameters that designers must consider when optimizing PC133 Registered DIMMS:

- CFB tuning to achieve 0ps CLK to SDRAM skew
- Output to output skew
- CLK to SDRAM skew variation

Registered SDRAM DIMM

Server/workstation/high-end PC platforms require very large DRAM memory size, typically more than 4 DIMM modules and more than 16 SDRAM chips per module. Because of overloading of the address/control/clock signals, unbuffered SDRAM DIMM modules cannot support such applications. Therefore, Registered SDRAM DIMM module products are required. A clock signal needs a PLL driver as a buffer to generate clock outputs to SDRAMs identical to the clock input with zero propagation delay. Since registered buffer drivers are used to buffer address/control signals, a register-buffered SDRAM DIMM is called a **Registered SDRAM DIMM**. Figure 1 shows the Registered SDRAM DIMM.

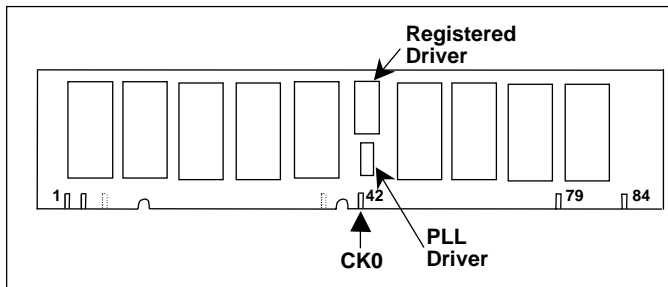


Figure 1. Registered 168-pin SDRAM DIMM

Only clock CK0 is used. The PLL driver generates 9 or 10 copies of clock CK0 on the DIMM module. A registered driver buffers the address/control signals.

The PLL driver PI6C2510-133 serves two purposes:

1. As a clock buffer for generating 10 copies of clock outputs from the single clock input CK0 at the DIMM edge connector (see Figure 2).
2. To adjust clock signal timing at the clock input pin of the SDRAM chips.

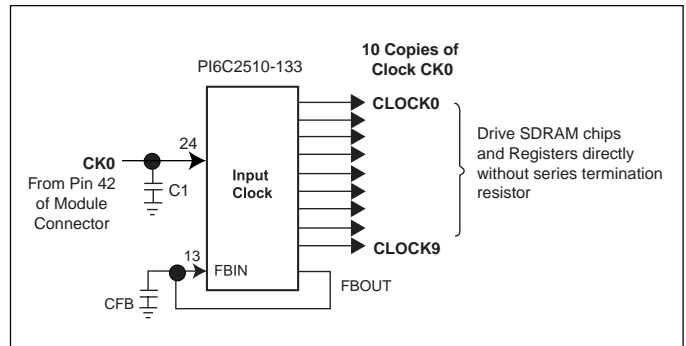


Figure 2. Block Diagram of PI6C2510-133

The objective is to assure that clock signals at all SDRAM chips are aligned with the module input clock CK0. This is to match clock timing at the SDRAM pin on the P133 **unbuffered** DIMM. Figure 3 shows the connection of the 2510-133 output clocks.

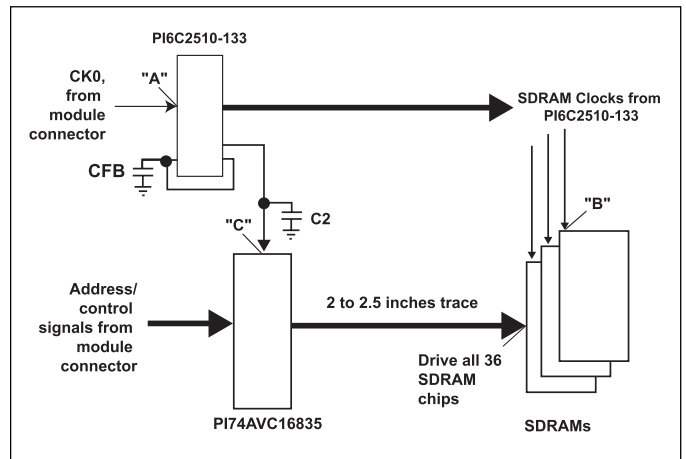


Figure 3. Address/Control Signals on a Registered DIMM Module

Align Clock Signals at SDRAM by CFB Adjustment

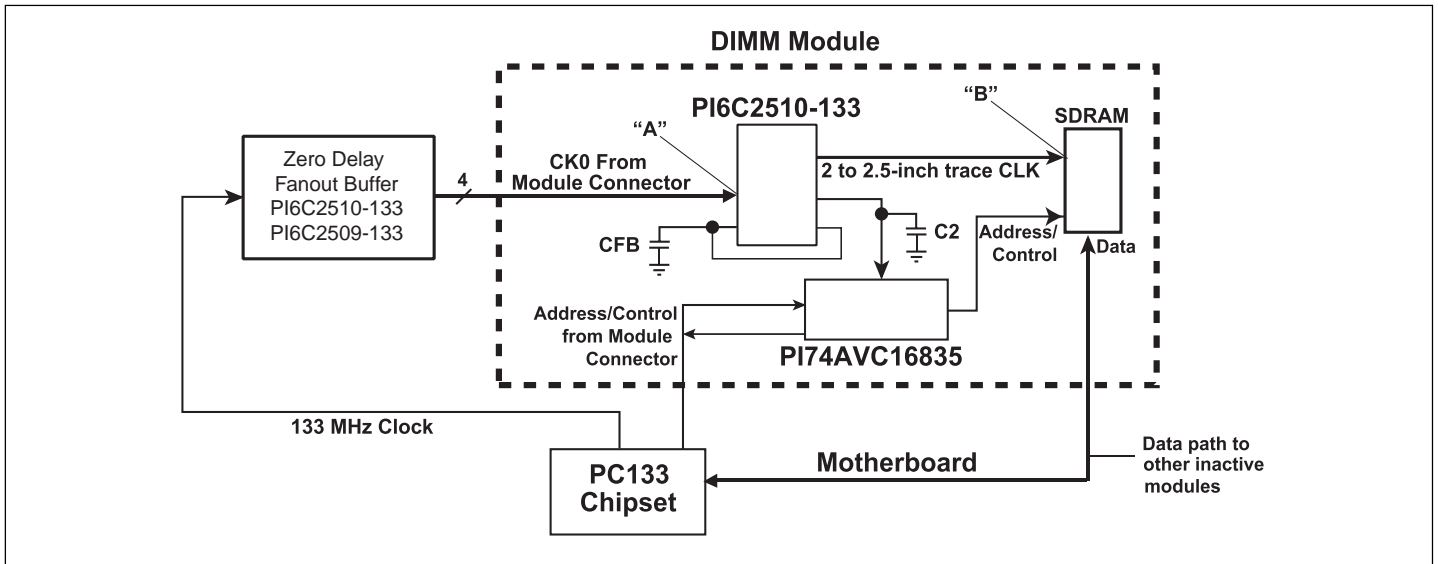


Figure 4. Clock Connection from PI6C2510-133 to SDRAM and Data Signal Path

In Figure 4, the clock timing at an SDRAM clock pin, point B, needs to be adjusted to align with the CK0 input clock timing at the 2510-133 clock driver, point A, within $\pm 100\text{ps}$ at 1.4V. This timing adjustment is accomplished by adjusting the value of the CFB feedback capacitor located near the feedback pin FBIN. It is important to determine the range of CFB values in which the DIMM is operational. Select a CFB value to provide enough margins for volume

production. A typical CFB value ranges between 5pF and 15pF, depending on the SDRAM-clock trace length on the module.

The CK0 (point “A”) to SDRAM Skew (point “B”) changes approximately 40ps/pF. See Figure 5 for assistance when adjusting CFB.

If a module layout design does not provide for the CFB capacitor, then it is very difficult to accomplish this objective, and the DIMM module operation becomes marginal.

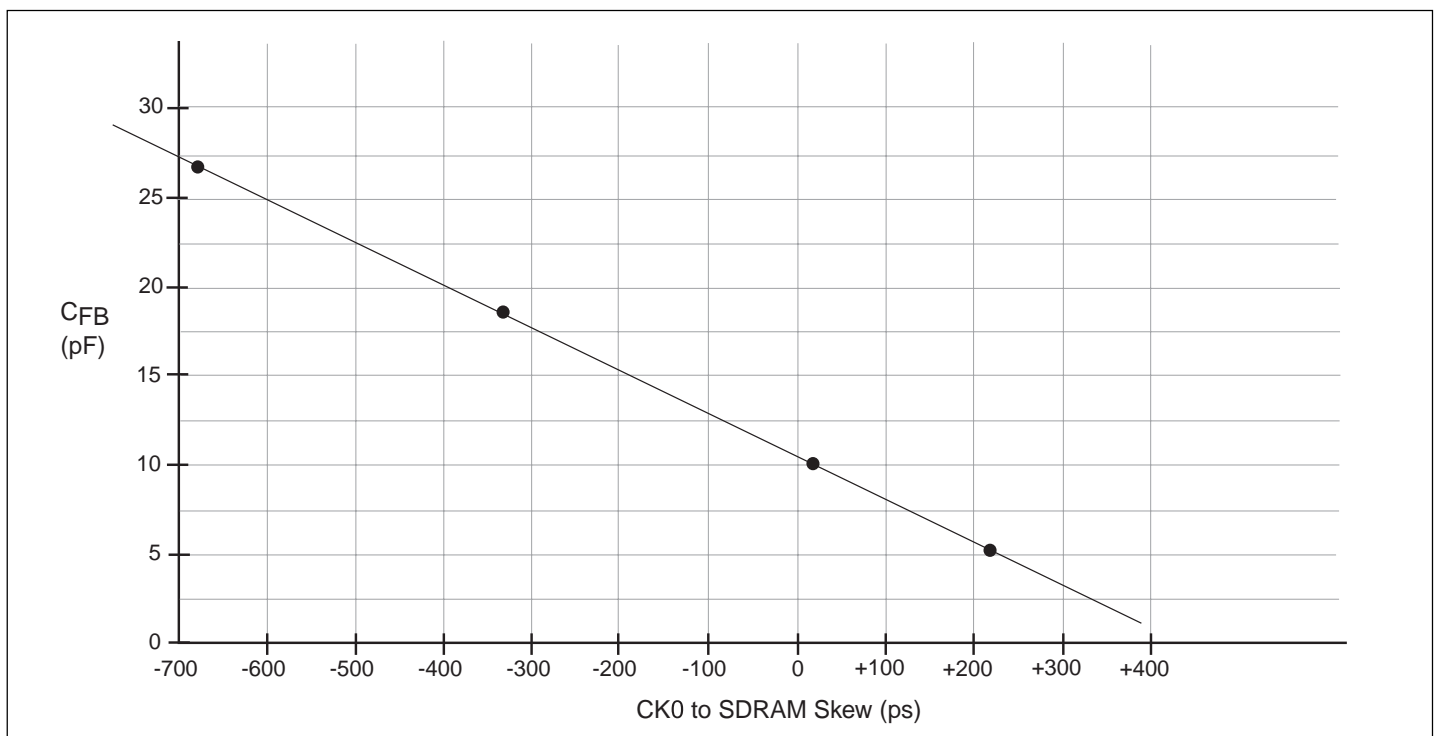


Figure 5. Graph of CK0 to SDRAM Skew vs. CFB

Output to Output Skew

With matched loads and equal trace lengths, output-to-output skew of the PI6C2510-133 is only 50ps. Measurements were taken at the SDRAM pins. Refer to Figure 6 for the actual scope traces of PLL outputs CLOCK0 to CLOCK9.

CLK to SDRAM Skew Over Process Variation

To ensure that the timing parameters will be met over process variation, devices from three different fab lots were placed in the DIMM. PI6C2510-133 CLK to SDRAM measurements were then taken without changing the optimal CFB of 10pF. Over the three fab lots CLK to SDRAM variations of 50ps were observed.

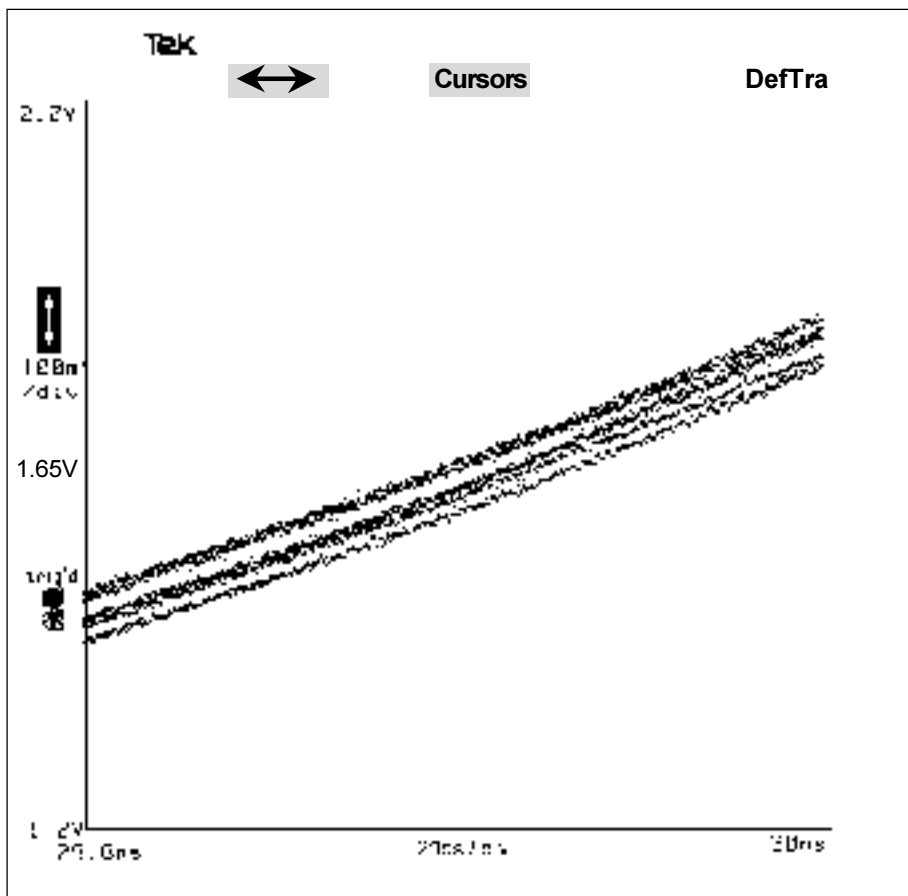


Figure 6. Digital Sampling Oscilloscope

Store Trace	Recall Trace	Clear Trace	Delete Trace	Vert Mag: Tra 100mV/div	
				Vert Pos: Tra 1.7V	
Store Setting	Recall Setting	Sequence Settings Off	Delete Settings	Remove/Cir Trace 8 STO7	Chan Sel Calcd Tra

Summary

The PI6C2510-133 meets and exceeds the PC133 SDRAM Registered DIMM, Design Specification, Rev.1.1. This Application Note 23 is intended to assist the designer when tuning the PLL for zero CK0 to SDRAM skew. Figure 5 can be used to determine the appropriate CFB feedback capacitor. All PLL measurements were taken at 133 MHz.

Equipment Setup

- 133 MHz input clock from CST Clock Evaluation Board
- TEK 11801C Digitizing Scope
- 64MB Planar DIMM, PC133 Raw Card "AA"