

Design Guidelines for PC100 Registered SDRAM Modules

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The PC100 Registered SDRAM module design has a tight timing budget. For reliable operation and volume production, two clock signals need to be tuned to meet the timing requirements of the data signal critical path and the address/control signal critical path. This application note describes how to perform the following:

- ❑ Alignment of the Clock Signal at the SDRAM chip for Data Signal Critical Path
- ❑ Alignment of the Clock Signal at the Registered Buffers for Address/Control Signal Critical Path
- ❑ Using Pericom's PI6C2509Q/2510Q 'quiet' PLL drivers for light load applications
- ❑ Verifying at the PC100 Platform level with a Spread Spectrum clock input and Windows NT.

Description of SDRAM DIMM Clock Signals

The most popular SDRAM modules are 168-pin DIMMs. Each module may have up to 36 SDRAM chips. Each SDRAM chip needs a clock input. To provide a clock to 36 SDRAM chips, the clock distribution circuit is a critical issue in DIMM module design. At 100 MHz, the clock period is only 10ns. The timing delay along the trace becomes very significant. The timing skew among such a large number of clock signals at the SDRAM chips becomes critical. To maintain clock signal integrity, the JEDEC specification requires a motherboard to provide four identical clock signals to each DIMM module at module pins 42, 79, 125, and 163 (see Figure 1). These four clock signals must be identical and driven by four separate clock drivers. If a motherboard has three DIMM sockets, then the motherboard must provide 12 identical clock signals driven by 12 clock drivers.

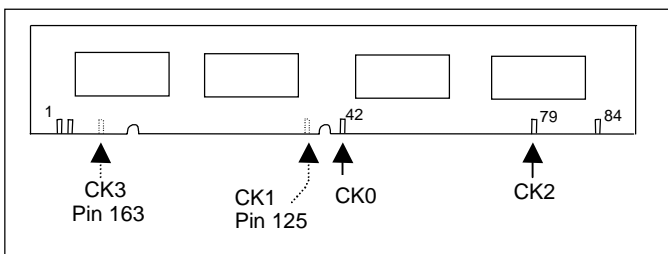


Figure 1. Unbuffered 168-pin SDRAM DIMM

To minimize the timing skew among the clock signals, the DIMM board layout design assures that the trace lengths of all clock signals from the PLL clock driver to each SDRAM chip are equal.

An unbuffered SDRAM DIMM module uses memory chips without buffer chips for clock/address/control signals. Each clock signal from the motherboard typically directly drives only 2 or 3 SDRAM chips on a module. JEDEC specifies each clock signal from a motherboard can drive up to 4 chips. Since there are only four clock signals from the motherboard, an unbuffered SDRAM DIMM module can have a maximum of 16 SDRAM chips.

Registered SDRAM DIMM

Server/workstation/high-end PC platforms require very large DRAM memory size, typically more than 4 DIMM modules and more than 16 SDRAM chips per module. Because of overloading of the address/control/clock signals, unbuffered SDRAM DIMM modules cannot support such applications. Therefore, buffered SDRAM DIMM module products are required. A clock signal needs a PLL driver as a buffer to generate clock outputs to SDRAMs identical to the clock input with zero propagation delay. Since registered buffer drivers are used to buffer address/control signals, a register-buffered SDRAM DIMM is called a **Registered SDRAM DIMM**. Figure 2 shows the Registered SDRAM DIMM.

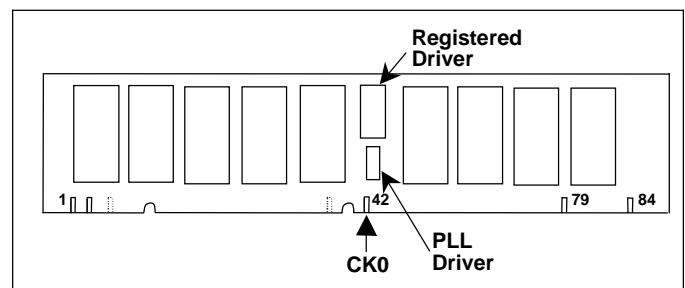


Figure 2. Registered 168-pin SDRAM DIMM

Only clock CK0 is used. The PLL driver generates 9 or 10 copies of clock CK0 on the DIMM module. A registered driver buffers address/control signals.

In a PC100 SDRAM DIMM design, the timing budget is very tight and can result in intermittent failures if the following two critical paths are not guaranteed with some margin. In the following description, "2509A" PLL refers to 2509A, 2509Q, 2510A and 2510Q. A "16835" Register refers to 16835, 162835, 16334, 162334, and 16836.

Align Clock Signals at SDRAM Chips for Data Signal Critical Path

The PLL driver 2509A serves two purposes:

1. As a clock buffer for generating 9 copies of clock outputs from the single clock input CK0 at the DIMM edge connector (see Figure 3).
2. To adjust clock signal timing at the clock input pin of the SDRAM chips.

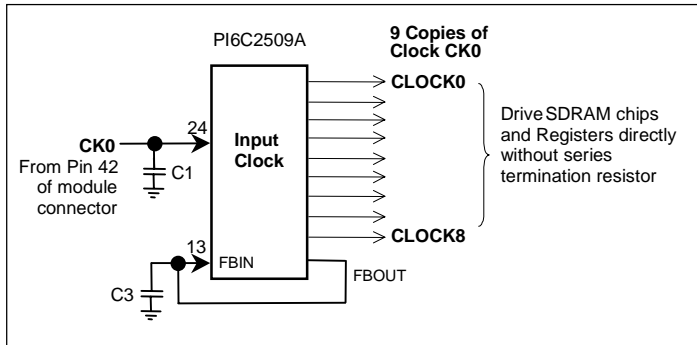


Figure 3. Block Diagram of PI6C2509A

The objective is to assure that clock signals at all SDRAM chips are aligned with the module input clock CK0. This is to match clock timing at the SDRAM pin on the PC100 *unbuffered* DIMM.

Figure 4 shows an SDRAM chip driving a data signal at read-data time. Here is the critical timing path:

$$T_{cosd} + T_{flt} + T_{scs} + T_{cskw} + T_{cjks} < 10ns$$

where

- Tcosd:** Max time from the clock at the SDRAM CLK pin (point “B”) to SDRAM output, 6.0ns max.
- Tflt:** Max flight time from SDRAM data output to Intel 440BX chipset
- Tscs:** Data setup time of Intel 440BX chipset
- Tcskw:** Skew from the module input clock CK0 (point “A”) to the clock at the SDRAM CLK pin (point “B”).
- Tcjks:** Clock jitter and the clock skew among the clocks at all SDRAM CLK pins.

Flight time, Tflt, is significantly long for the following reasons:

1. Data output of an SDRAM chip is a weak driver: Ioh of only 4mA at 2.4V and Iol of 4mA at 0.4V.
2. Because corresponding data bit paths of all DIMM modules are connected, the data output driver of an SDRAM chip also drives data paths of other inactive DIMM modules.

If the C3 capacitor is not tuned, the skew Tcskw between the module input clock CK0 (point “A”) and the clock at the SDRAM CLK pin (point “B”) could be several nanoseconds. The goal is to reduce Tcskw to zero.

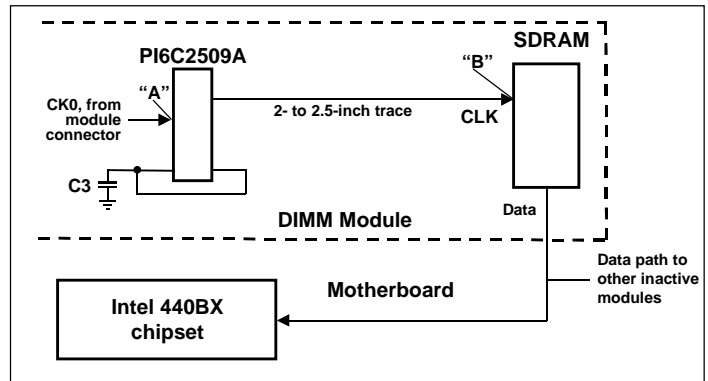


Figure 4. Clock Connection from PI6C2509A to SDRAM and Data Signal Path

Tuning the Clock by Adjusting C3 Capacitor

In Figure 4, the clock timing at an SDRAM clock pin, point B, needs to be adjusted to align with the CK0 input clock timing at the 2509A clock driver, point A, within ±50ps at 1.4V. This timing adjustment is accomplished by adjusting the value of the C3 capacitor located near the feedback pin FBIN. It is important to determine the range of C3 values in which the DIMM is operational. Select a C3 value to provide enough margins for volume production. A typical C3 value ranges between 5pF and 15pF, depending on the SDRAM-clock trace length on a module.

If a module layout design does not provide the C3 capacitor, then it is very difficult to accomplish this objective, and the DIMM module operation becomes marginal.

A high-speed oscilloscope, with a sampling rate of at least 1 GHz, is required to check a 100 MHz clock signal. An oscilloscope of 4 GHz sampling rate is preferred. To see the real clock waveform, use an active probe with a short ground connection.

Align Clock Signal at Registered Buffers for Address/Control Signal Critical Path

The Registered Buffer ALVC16835 is used to provide a buffer for the control/address signals.

As indicated in Figure 5, the Registers drive address/control signals to all 36 SDRAM chips. Here is the critical path:

$$T_{corg} + T_{flt} + T_{ssd} + T_{cskw} + T_{cjks} < 10ns$$

where

- Tcorg:** Max time from the clock at the Register CLK pin (point “C”) to Register output, 2.5 to 3.0ns.
- Tflt:** Max flight time from Register output to all SDRAM input pins, 3.4ns to over 4.0ns.
- Tssd:** Address/control signal setup time of SDRAM chip, 2.0ns.
- Tcskw:** Skew from module input clock CK0 (point “A”) to Register CLK pin (point “C”).
- Tcjks:** Clock jitter and clock skew among Register clock pins

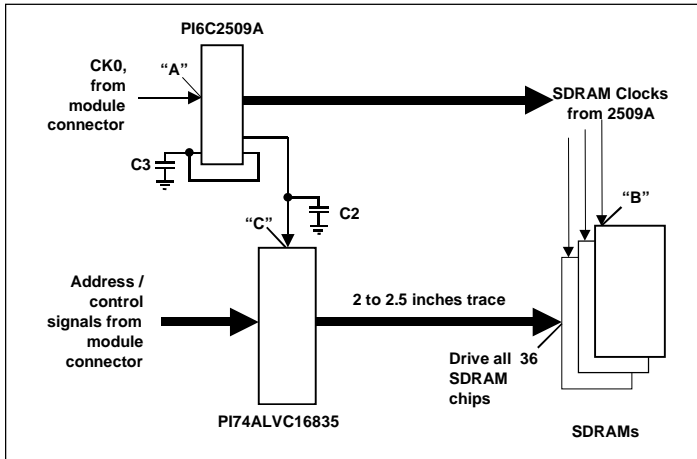


Figure 5. Address/Control Signal Critical Path on a DIMM module

This path is critical, with almost no margin even if $T_{csw} = 0$. To gain additional margin, it is recommended that T_{csw} be adjusted to a negative value, -250 ± 50 ps.

Tuning the Clock by Adjusting C2 Capacitor

Because the 2509A PLL and the registers are located nearby on the module, clock traces from the 2509A PLL to the registers are typically much shorter than the clock traces from the 2509A PLL to the SDRAM chips. In Figure 5, the clock timing at Register clock pin, Point C, needs to be adjusted to “lead” the CK0 input clock at the 2509A PLL, Point A, within $-250\text{ps} \pm 50\text{ps}$ at 1.4V (see Figure 6). This timing adjustment is accomplished by adjusting the value of C2 located near the registers. If a module layout design does not provide the C2 capacitor, then it is very difficult to accomplish this objective, and the DIMM module operation becomes marginal. A typical C2 value ranges between 5pF and 15pF, depending on the register-clock trace length on a module.

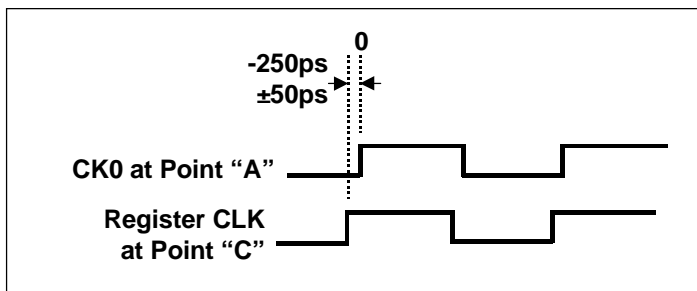


Figure 6. Register CLK at Point “C” leads CK0 at Point “A”

Use Pericom’s PI6C2509Q/2510Q ‘Quiet’ PLL Drivers for Light Load Applications

Pericom's PI6C2509A/2510A parts provide a strong output drive ideally suited for heavy load applications.

Since each clock signal may drive only 2 SDRAM chips on some DIMM modules, Pericom offers the PI6C2509Q/2510Q parts for such light load applications, resulting in ‘quieter’ operation without clock signal undershoot/overshoot.

Verify at PC100 Platform Level with a Spread Spectrum Clock Input and Windows NT

After passing a module tester, a PC100 SDRAM DIMM should be also tested at a PC platform with Spread Spectrum enabled. The PC platform should include the following:

1. A 100 MHz Bus Intel 440BX motherboard with Pentium II of at least 350 MHz

A 100 MHz Bus Intel 440BX motherboard that will automatically run at 66 MHz bus if a Pentium II of lower than 350 MHz is used. Because some customers use Pentium II processors of less than 350 MHz, a PC100 SDRAM DIMM module should pass at 100 MHz bus mode as well as 66 MHz bus mode.

2. Microsoft Windows NT Operating System

Windows NT is more stringent than Windows 95 for testing DIMM modules.

3. Enabling Spread Spectrum and running for many days during pilot-run testing of modules.

For EMI reduction to pass FCC requirements, the clock generators for new generation PC100 platforms provide clock signals with spread spectrum to CPU and SDRAM DIMM modules.

The spread spectrum feature should be enabled during pilot-run testing of the DIMM modules.

