

General Routing Techniques with Emphasis on PI6C10X Clocks

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Pericom's advanced process technology provides market specifications for Skew, Jitter, and EMI. In addition, Pericom's devices provide lower power consumption, smaller board space, lower operating temperature, and lower cost requirements.

To avoid poor quality clock transmission, it is very important to consider certain clock layout and routing techniques. This application note is concerned with power supply filtering, bypassing, and routing techniques for crystal, ground and power supply. Since these techniques concern power and ground, they apply to almost every clock. The application note discusses some of the existing

terms and problems faced by design engineers when using clocks in their systems. It also discusses the techniques to eliminate or alleviate such problems.

Jitter

The deviation in clock output transitions from their ideal positions is called Jitter, measured Cycle-to-Cycle. Jitter is the measure of the difference in the period of successive cycles of a continuous clock pulse (see Figure 1). The aim of this application note is to show techniques that reduce Jitter and eliminate their causes.

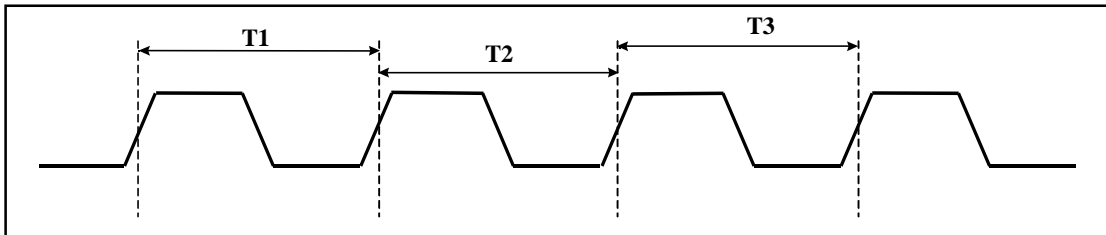


Figure 1. Cycle-to-Cycle Jitter = $T2 - T1$, $T3 - T2$

Long Term Jitter is the difference in a clock output transition from its ideal position over many cycles (10 to 20 microseconds, see Figure 2). To reduce Jitter we need to understand that Power

Supply Noise, Ground Bounce, PLL, Random Thermal Noise, and Random Mechanical Noise are its causes. Eliminating ground bounce and reducing power supply noise significantly reduces Jitter.

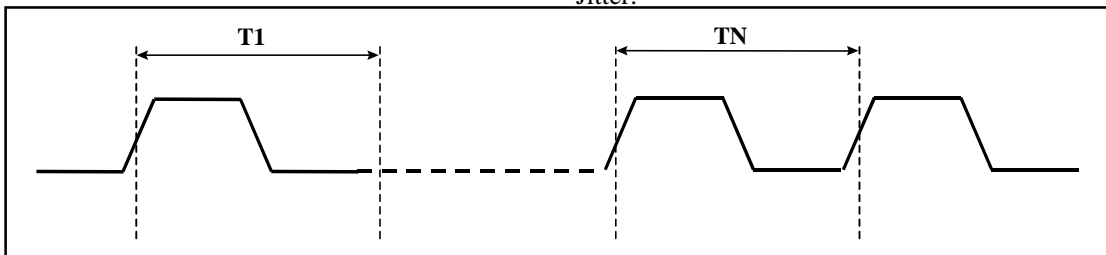


Figure 2. Long Term Jitter = $TN - T1$

Period Jitter is the measure of maximum change in a clock's output transition from its ideal position during a single period.

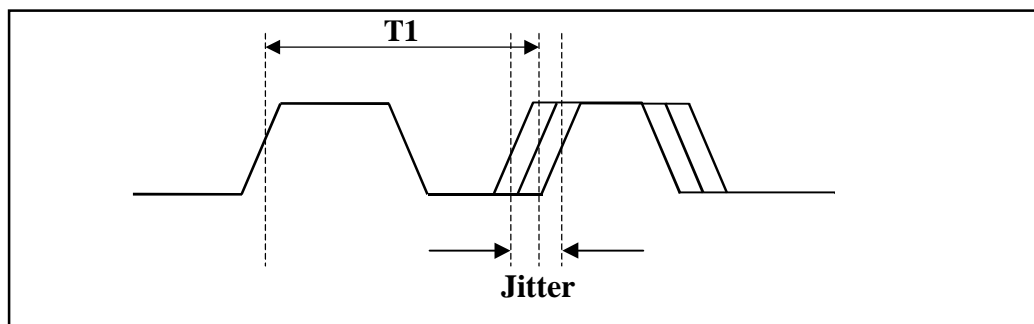


Figure 3. Example of Period Jitter

Reducing Power Supply Noise

Filtering method and bypassing are the most frequent ways of reducing the power supply noise. Placing a large tantalum capacitor connected to the source eliminates power supply ripple and current surges. For high frequency ripple elimination, small capacitor (0.1mF) on every Vdd of clock generator significantly reduces the high frequency ripples. To eliminate the noise coupling effect, no high frequency signals should be routed around or under the clock generator. We will discuss these techniques in more detail.

Eliminating Ground Bounce

Reducing the number of output loads can significantly eliminate ground bounce. Large and/or multilevel PCB Ground Planes also help to reduce ground bounce. Do not short individual ground pins together. Always connect each separately to a large ground plane. Large output currents also cause ground bounce. Limiting the output current can reduce ground bounce very effectively. If possible, always disable unused outputs.

Board Skew

Unequal trace lengths and loads cause the board skew independent of the skew generated by the buffer. To minimize board skew the design should have equal trace length and loads as much as possible.

Output Skew

This is the difference between two concurrent clock outputs that originate from a single input. Skew is mainly the variation in arrival time of two clock signals that are specified to occur at the same time. Skew is composed of the output skew of the driving device and the variation in the board delays caused by the layout variation of the output traces. Skew directly affects system margins by eroding the predictability of the arrival of a clock edge. Because elements in a synchronized system require clock signals to arrive at the same time, clock skew reduces the time when information can be passed from one device to the next. As system speeds increase, clock skew becomes a larger portion of the total cycle time. Clock Skew can be as much as 20% of cycle time. When cycle time approaches 15ns or less clock skew becomes increasingly important. For high-speed systems, skew can only consume 10 percent of cycle time. Skew as a result of clock driver is called intrinsic skew and skew as result of layout is called extrinsic skew.

Overshoot and Undershoot

Clock generators have low output impedance. When a device drives a load with large input impedance while its own output impedance is low, there will be a mismatch between the low impedance source and high impedance load. Most often when the traces are long such a condition is significantly worsened. These cause voltage reflections resulting in high voltage overshoot on the rising clock edge and voltage undershoot on the falling clock edge. Proper termination techniques will help eliminating these conditions. We will discuss termination schemes in more detail.

Solutions to Routing Problems

Reducing RF Currents

To provide an efficient path for RF currents to ground place a localized ground plane under the clock generator. The inside PCB ground plane could be two or three levels away and may not be sufficient for RF current path.

Xin and Xout Pins (focus on PI6C10X)

In the PI6C10X, the Xin and Xout pins are the input reference clocks. In the majority of designs, a parallel resonant quartz is connected to Xin and Xout pins. The device already includes the parasitic and loading capacitors that are connected to Xin and Xout and ground. In designs where there is already a clock available, this clock signal is connected to Xin pin directly and Xout is left unconnected. The leads of the Crystal Oscillator connected to Xin and Xout pins should be as short as possible since the Xin pin is high impedance and is highly sensitive to noise. To prevent inductive and capacitive coupling any other clock signal should not be close to Xin and Xout signals.

Bypass Capacitors

To eliminate the majority of the noise, the design engineer must consider these steps. Each VDD should have a minimum of 0.1 μ F capacitor to ground to eliminate high frequency noise. Rising clock edges that cause current spikes from PCB Power and Ground planes causes the high frequency noise. To allow for better power bypassing, the power and ground should be as close as possible in the PCB layers. All decoupling capacitors must be placed on the same side as the component on the PCB. For the best performance, we strongly recommend high quality, monolithic, ceramic, surface mount capacitors with low ESR. These capacitors must be placed as close to the device pins as possible. As shown in Figure 4, typically a 0.1 μ F capacitor for every power supply pin of the clock generator is sufficient. However, for higher frequency noise, capacitors in the range of 200pF to 2.8nF are more suitable. The best performance is obtained with a large and small chip capacitor connected as closely as possible to the supply.

Noise Reduction Circuit

It is highly recommended to use a noise reduction circuitry on entering power supply line. This circuit consists of a resistor and a capacitor as shown in Figure 4. This circuit is used to decouple the power rail from the system supply. The resistor value should be around 2.7 ohms. This circuit in effect reduces the power supply variations that may cause destabilization. Destabilization usually presents itself in the form of Jitter. In the severest form it may even cause loss of PLL locking. In production, however, it is possible to remove this resistor if it does not cause problem. Tantalum capacitors with values between 10 μ F and 100 μ F can be used to eliminate power supply destabilization. This condition mainly is seen when the clock generator is switching all outputs at the same time with maximum capacitive load.

The switching noise generated by the clock generator should be decoupled to PCB ground planes. This noise is being radiated through the power connection to the board power supply. To block this high frequency noise and to accomplish this decoupling, tantalum capacitors and a Ferrite Bead are used to block the high frequency noise. The Ferrite Bead in essence isolates the main power plan of the board from the clock generator power plane. This method eliminates the noise generated by the clock generator from reaching the main power supply plain. A minimum of 1.7 Henries is recommended for this Ferrite Bead, however, the bigger the Ferrite Bead the better blocking is accomplished. Indeed, there is

always a trade off with space. The Ferrite Bead must be capable of providing the rated DC current to the VCC plane. Also DC impedance of the Ferrite Bead must be very close to zero. The impedance of the Ferrite bead, however, at the clock frequency must be very high. This is typically greater than 50 ohms under loaded conditions with DC current flowing through it. With these conditions met, the Ferrite Bead will then present a large impedance at the clock frequency and will prevent noise due to clock harmonics from flowing to the PCB. Figure 5 shows the High Frequency Power Bypassing Schematic. Figure 6 shows the PCB layout and the place for the Ferrite Bead.

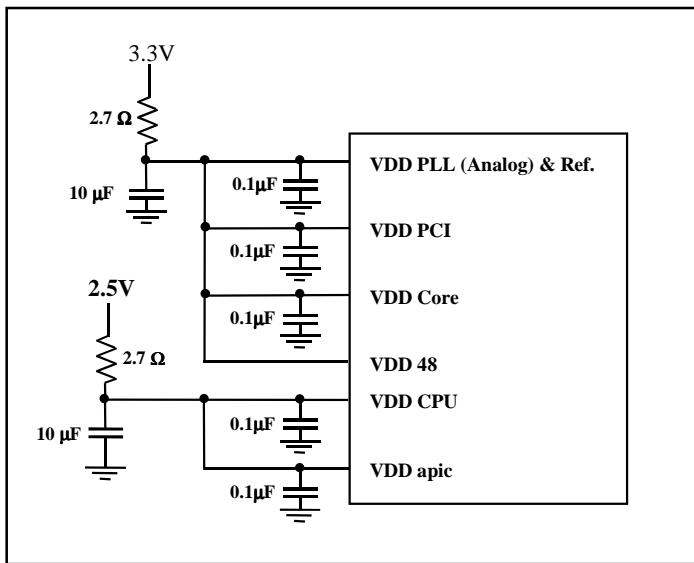


Figure 4. Low Frequency Power Bypassing Schematic

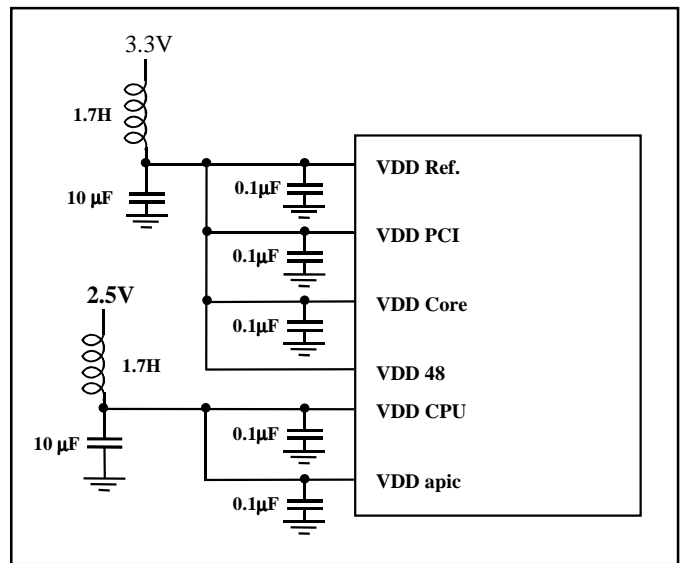


Figure 5. High Frequency Bypassing Schematic

Clock traces can easily become antennas. 100 MHz clock running through a narrow trace can radiate EMI and affect the FM radio sitting next to the system. As is evident, 100MHz is right at the middle of the FM radio spectrum. The way to further decrease the EMI radiation is to guard against improper loading and mismatches. To practically eliminate this problem, the source impedance of the clock driver should be matched in impedance to the load and the circuit trace. Most often a series termination is placed as close as possible to the source.

Theoretically the output impedance of the clock driver plus the value of the termination should be equal to the impedance of the PCB transmission line. If there is an impedance mismatch between the low-impedance source and high-impedance load, voltage reflection can occur from the load. This will result in overshoot and undershoot of the signal. The output impedance of the clock driver ranges from 20 to 30 ohms. To match this with a 50-ohms transmission line, a 30 to 20 ohms damping resistor should be chosen. The drawback is that the termination resistor reduces the amount of current and in effect reduces the clock waveform rise and fall time. It is very important to choose a proper value of damping resistor since any excessive voltage drop may increase the clock jitter.

To reduce ground bounce that causes jitter, a full ground plane under the device is necessary. All bypass capacitors are connected to this ground plane. Each ground pin should be connected to the ground plane individually. Daisy chain grounding should not be practiced since it allows sharing the ground path. No high frequency signal should be routed under the device since high frequency clocks tend to capacitively and inductively couple into the device and cause jitter in the PLL. Figures 6 and 7, shown below, illustrate the recommended PCB layout for the power supply bypassing the clock generator and the CK100 clock buffer, respectively. This method dramatically reduces the noise that may enter the PLL and cause jitter. The value of the resistor should not be too high to stop the device from proper functioning.

The PI6C18X Clock Buffer

The PI6C18X is a buffer device that removes large switching current from the actual clock generation device. The PI6C18X, however, introduces a delay of up to 5ns. The Intel chipset and new chipsets resolve this problem by providing the clock to the PI6C18X. The chipset can read the exact amount of the delay and can compensate for this delay. In effect the chipset adjusts the SDRAM timing to optimize the relationship between CPU and SDRAM timing.

EMI Reducing Capacitors

If the amount of EMI is still very high in a system, it is possible to alleviate this condition even further by using a special type of capacitor. The EMI reducing capacitor is mainly used on the output clocks to round the falling and rising edges of the clock and hence reduce the radiation from sharp edges. The EMI reduction capacitors usually range from 4pF to 25pF. They are placed very close to

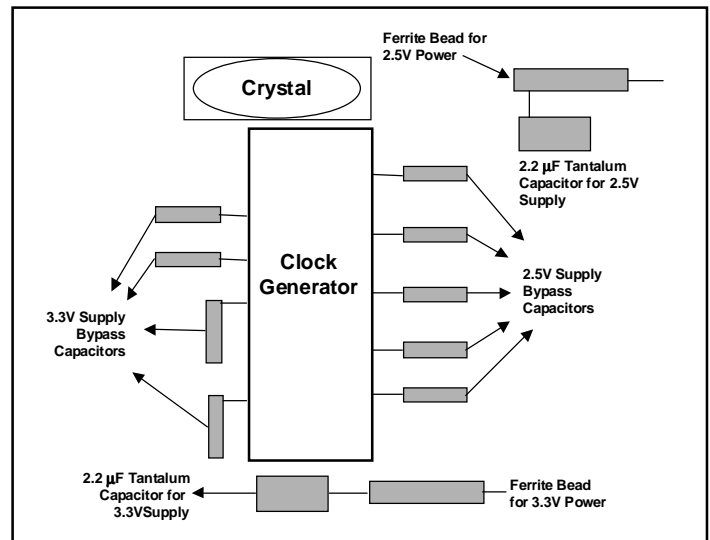


Figure 6. PCB Layout and Routing

terminating resistors between the resistor and the load.

No connection should be made to clocks that are not used. No termination is recommended for unused clock pins. Since these devices are CMOS, they draw large impulse current. If the power supply bypassing is not adequate, the noise as the result of these transitions may enter the device analog section and increase the jitter. Where possible, disable unused clock outputs.

Ground Plane Localization

The entire board must have a separate ground plane, however, it is strongly recommended to localize the ground plane for the clock generator. This localized ground plane is then connected to the main board ground plane through Vias and device pins.

Other Routing Issues

The clock must be placed near the center of the board and near a chassis ground. Clock traces should not intersect each other. All clock signals must be hand routed before any other signals.

More tips on routing and connections: Do not use 90 degree angles when routing clock traces. If possible, always use curvy traces. Do not route any other signals below the clock generator. A solid ground plane must be placed on the layer adjacent to a clock trace routing layer. Vias should be avoided on clock signals. Vias cause reflection by changing trace impedance. Vias should not cause discontinuities either. For low skew, signal traces must be of matched length and loading, and, if possible, identical. If certain signals are supposed to have certain skews with each other, their trace length must be equal. Do not use T connections. For minimum skew, use one load per clock output.

Board Layout for Reducing EMI and Preserving Signal Integrity

It is recommended that you calculate the capacitive loading and compensate with a series damping resistor and/or end termination.

Do not locate clock signals near I/O areas. To minimize reflections and ringing keep trace impedance balanced and short. It is highly recommended that you rout clock traces on one routing plane only. At all times this layer must be adjacent to a solid image plane. It is better to create localized ground and VCC planes on the top layer of the PCB. The localized ground plane should be beneath the chip and the VCC plane surrounds the chip. These planes provide a path for RF currents to return to ground.

Summary

Pericom has started a clock journey. We have focused on clocks that are best suitable for high-performance systems designs. These

are both clock generators and clock buffers (drivers) that have excellent attributes, tighter timing, lower power consumption, lower operating temperature, and smaller packages. Lowest clock skews guarantee better designs and optimum performance.

This note covers the basic important clock terms and their effect on system performance. Pericom is committed to developing products that meet emerging market requirements and needs.

References

1. Montrose, M.I., Printed Circuit Board Techniques for EMC Compliance." IEEE Press, 1996
2. Johnson, H.W, and Graham, M., "High Speed Digital Design." Prentice Hall, 1993.

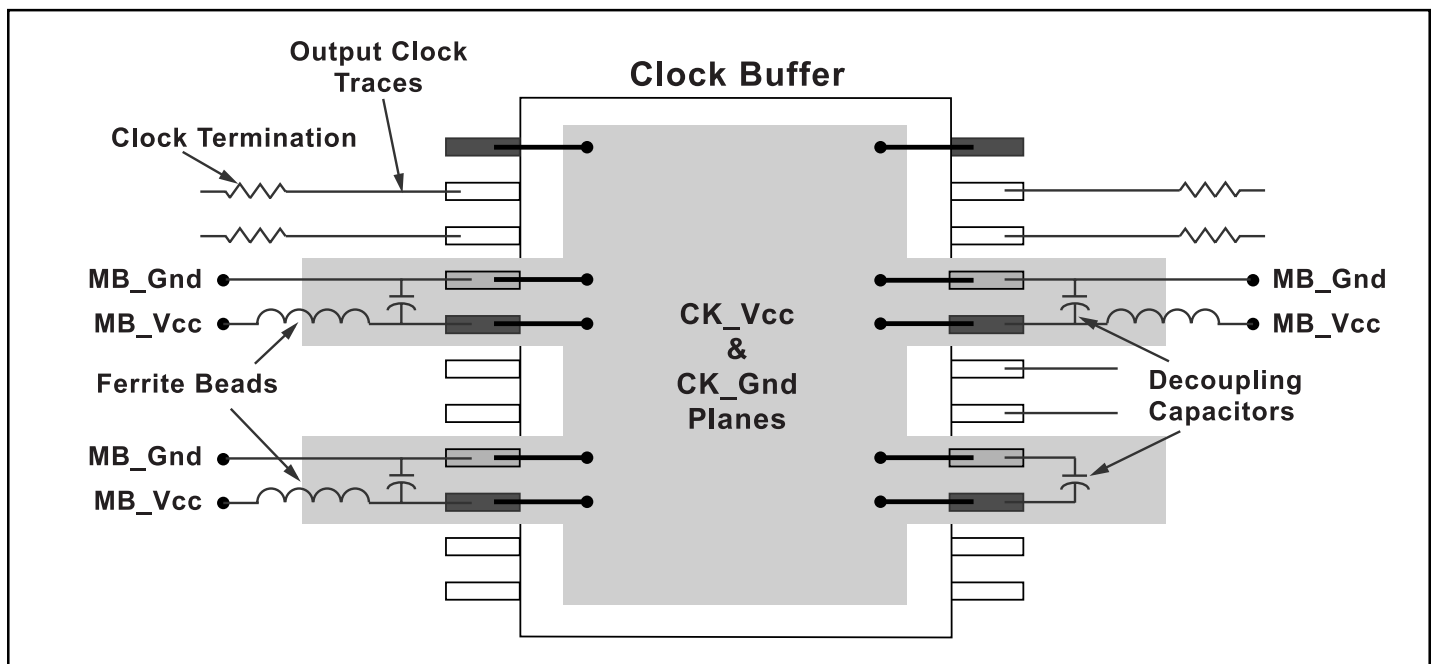


Figure 7. CK100 Clock Buffer EMI Guideline

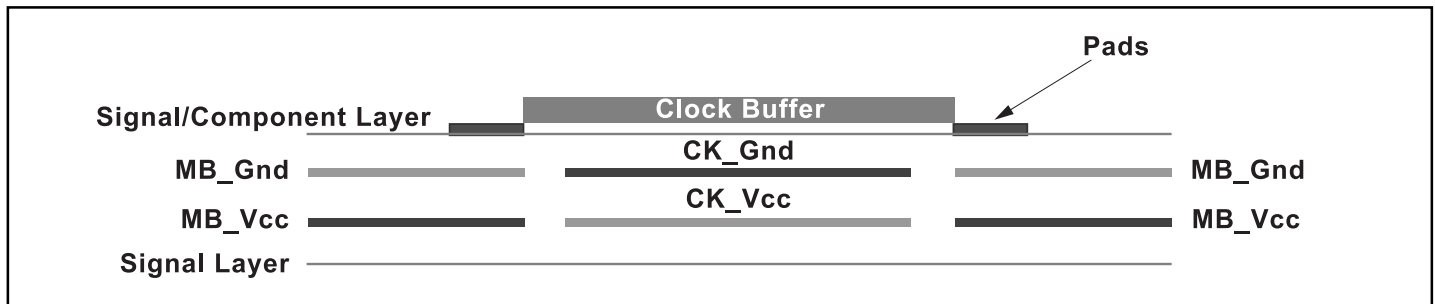


Figure 8. CK100 Clock Buffer EMI Guideline (Cross Section)

