Clock Basics

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Purpose

The purpose of this document is to provide the reader with information on clocks, their related terminology and criteria that need to be considered prior to making a selection of the device. It is meant for the beginner as well as for enhanced users. Besides the definitions, the document highlights clock based devices available from Pericom, parameters that are taken into consideration by users of these devices, and useful references.

SiliconClock

SiliconClock is a broad-based term used for the family of clocks and clock based devices offered by Pericom Semiconductor Corporation. Some of the IC devices in this family are high-performance 3.3V and 5V clock distribution circuits, PLL-based zero-delay clock buffers, and clock generators that are used in PC, printer, networking, datacom and telecom applications.

SuperClock™

As more and more applications require high frequency signals to be distributed more precisely, the “skew” parameter of an input clock could cause problems. The delay caused due to the skew can erode the timing margin in a typical system. Pericom provides a solution to this problem by offering the SuperClock. One of the key features of the SuperClock is that it provides adjustable skew and is intended for high-performance computing or networking applications.

For a complete description of different SuperClock products, please visit www.pericom.com.

Clock Drivers

For most applications that use clocks or clock generators, a clock buffer or driver is also required. Typically, the function of this driver is to drive one input to several outputs. In the past, a time delay (propagation delay) has usually been associated with such devices. Pericom provides several families of clock drivers, of which some have relatively no time delay (hence referred to as zero-delay) between I/O.

For example, the PI6C2308A clock buffer has a very low input to output propagation delay (<150ps) which helps in reducing the overall time taken for a clock signal to be delivered. Most of these devices are available for inputs of either 5V or 3.3V. Some of the other features of the clock buffers are low skew, multiple output banks, and low jitter.

Specific information on clock drivers can be found by visiting www.pericom.com.

Terminology

Jitter

For most clock devices, jitter is a time based error and can be seen as the deviation of the output from its ideal phase or frequency. In a typical application this will be seen as phase noise and may even get amplified if multiple stages are involved in the design. In order to overcome this situation, PLL based clocks are used. Jitter is typically described as cycle-to-cycle (i.e. it is the difference in the clock's period between two consecutive cycles). Jitter is expressed in units of ±ps. This is because it can be either leading or lagging from the ideal output waveform.

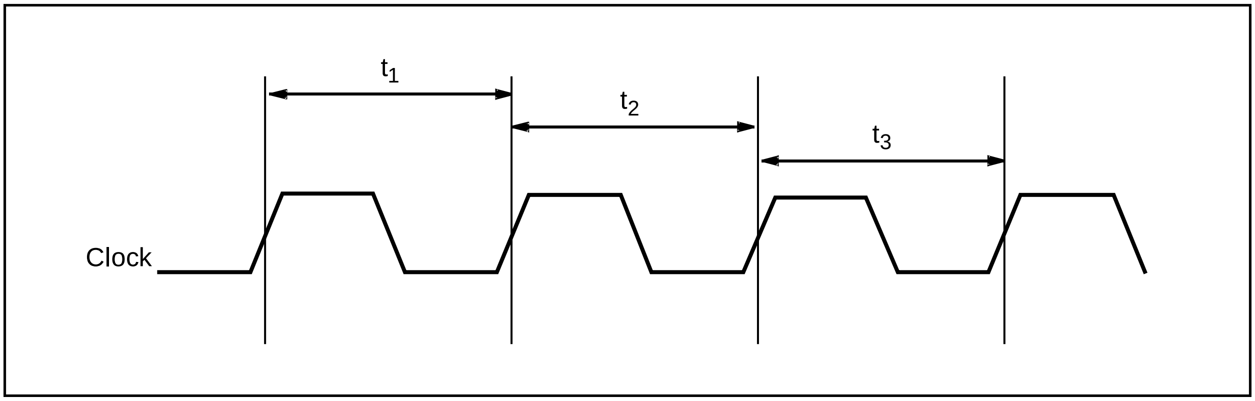

Figure 1. Cycle-to-Cycle Jitter = T2-T1, T3-T2

Period Jitter

Period Jitter can be defined as the measure of maximum change in a clock's output transition from its ideal position during a single period. This type of jitter is considered in high-speed designs. It is measured as:

Tjit (per) = Tcycle – 1/Fo,

where Fo is the frequency of the input signal. Consider an input clock signal of 20 MHz being applied to a driver. If the output on the driver has a measured period (Tcycle) of 51ns on the oscilloscope then,

Tjit = 51 –1/20Mhz =1ns

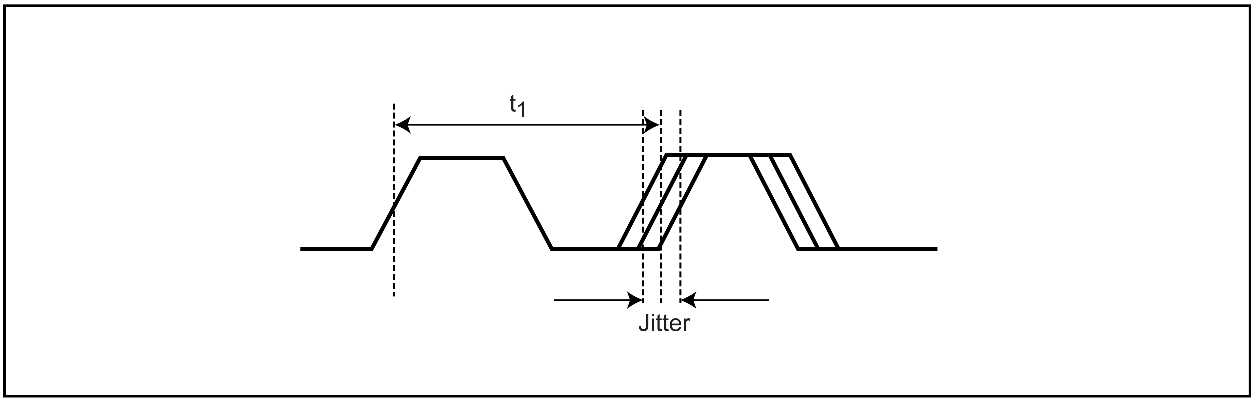

Figure 2. Period Jitter

Half-Period Jitter

Half-Period Jitter is the measure of maximum change in a clock's output transition from its ideal position during one-half period. This type of jitter is considered in double data rate (DDR) transfer applications. It is measured as:

Tjit (hper) = Thalfperiod – 1/2Fo, where Fo is the frequency of the input signal.

Considering the above example of a 20 MHz clock and a 25.1ns half cycle, the half-period jitter will be measured as:

Tjit(hper) = 25.1 – 25 = 0.1ns (or 100ps)

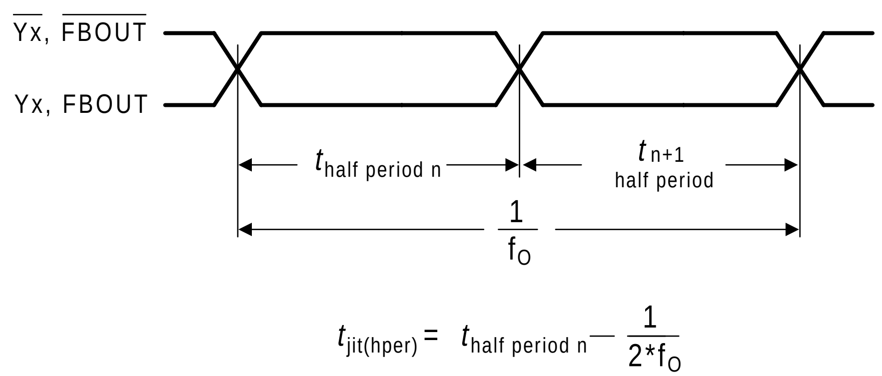

Figure 3. Half-Period Jitter

Skew

Skew is the variation between the rising edge of one signal versus the rising edge of another signal. It can also be measured between the falling edge of one signal versus the falling edge of another signal.

Output-to-output skew

In clocks or clock-based devices, skew is measured between two outputs and is also specified in the data sheets as tsk(o): output-to-output skew of the same device.

Note: The conditions for the two outputs should be the same (load, trace lenght, ect.).

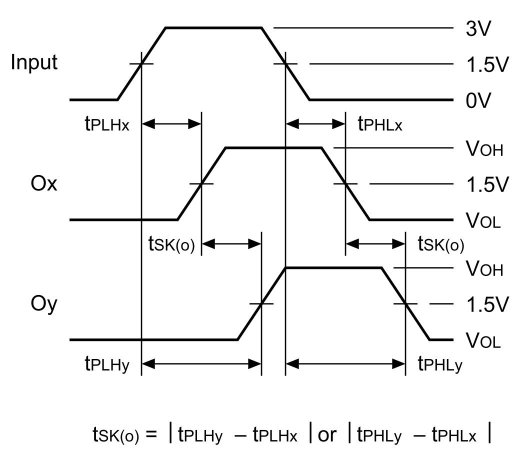

Figure 4. Output-to-Output Skew

Part-to-Part skew

The skew between two outputs of two similar types of devices under similar operating conditions (reference clock, V_{CC}, temperature, load, trace lenghts, etc.) is referred to as the part-to-part skew. As in the case of measuring output-to-output skew, this skew can also be measured between the rising edges or falling edges of the two output signals.

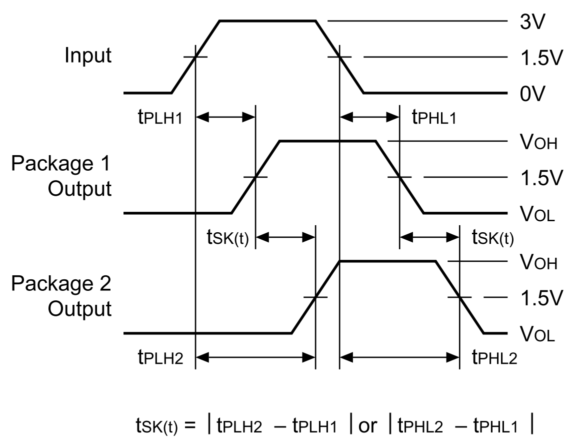

Figure 5. Part-toPart Skew

Output Impedance

Output impedance is the impedance seen on the output of the clock or driver. However, this is one of the characteristics that designers need to know for their layout design. Depending on the impedance of the transmission line, reflections may be seen. Therefore, it is important to have appropriate termination impedance that matches the output impedance of the device.

In Figure 6 below, the sum of the output impedance of the driver and the series resistor must be equal to the characteristic impedance of the trace (Zo). This Figure shows series termination, which is a common termination technique.

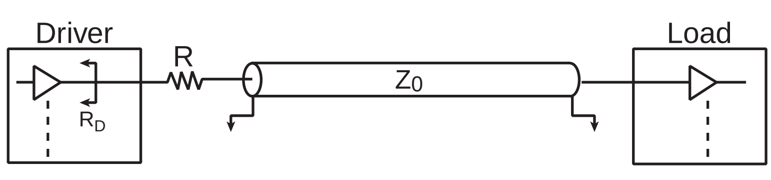

Figure 6. Matching output impedance using series termination

Ringing

Ringing is a signal sampling or timing related problem and can be defined as the overshoot or undershoot of a signal a number of times following a logic level transition. It can occur due to several reasons such as lack of termination resistors, reflections, device rise time, line length, line impedance mismatching, discontinuities, and loading.

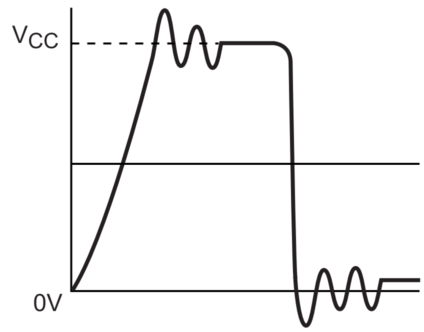

Figure 7. Ringing in a clock circuit

Crosstalk

Crosstalk is interference caused by signals from one circuit being coupled into other circuits. On PCB routing, special consideration is given to high frequency signals such as clocks to ensure that crosstalk does not affect them much.

Termination

A component (typically a resistor or diode) added at the end of the line to establish a relationship of the load or source impedance with line impedance. Some commonly known termination techniques are series termination, parallel termination and Thevenin termination. For more techniques on terminating transmission lines, please refer to Pericom's application note 22, "Solutions to current high-speed board design."

Selecting a Clock driver

Since the success of the system depends on the performance of the clock circuit, it is important to properly select the clock driver. Some factors to consider are:

A) Power dissipation should be low

B) If zero delay is required in the driver, choose a PLL based clock.

C) Jitter, skew, Propagation delay, rise times, fall times and other switching characteristics need to be considered. Most data sheets will provide this data with respect to certain loading conditions. Since, clock drivers are faster and dissipate less power when driving lighter loads, the given data should be considered with respect to individual design in mind.

References

1. Johnson, H.W. and Graham, M. "High speed digital design." Prentice Hall, 1993.
2. Konsowski Stephen and Helland Arden, "Electronic packaging of high speed circuitry." McGraw Hill, 1997.
3. Ginsberg, Gerald, "Printed circuit design" McGraw Hill, 1991.
4. Tisani, Mohamad, "Solution to current High-Speed Board Design." Pericom Semiconductor Corp., AN22, 2000.

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