

Real Design Issues for Clock Buffers for Networking and PC Applications

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Introduction

Advanced processors from Intel corporation run on clocks with a frequency of 100 MHz, which translates to a period of 10ns. These clocks are also used to drive other processors and to synchronize the transfer of data between other components such as chipsets,

PCI Bridges, PCI and ISA slots, Super I/O, graphic devices, and main memory. Figures 1 and 2 show block diagrams of clock distribution for a system with dual processors.

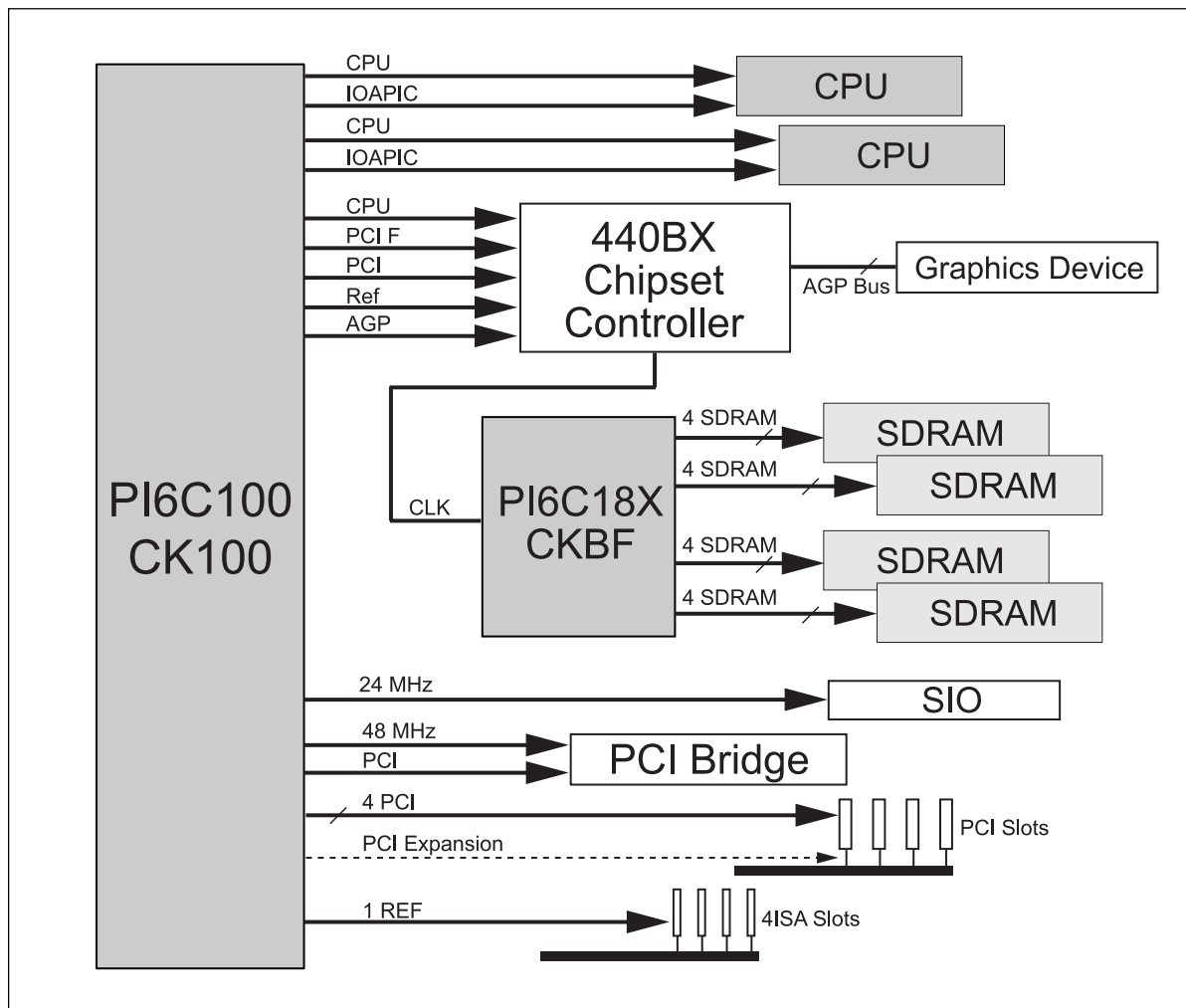


Figure 1. Clock Distribution for a System with Dual Processors

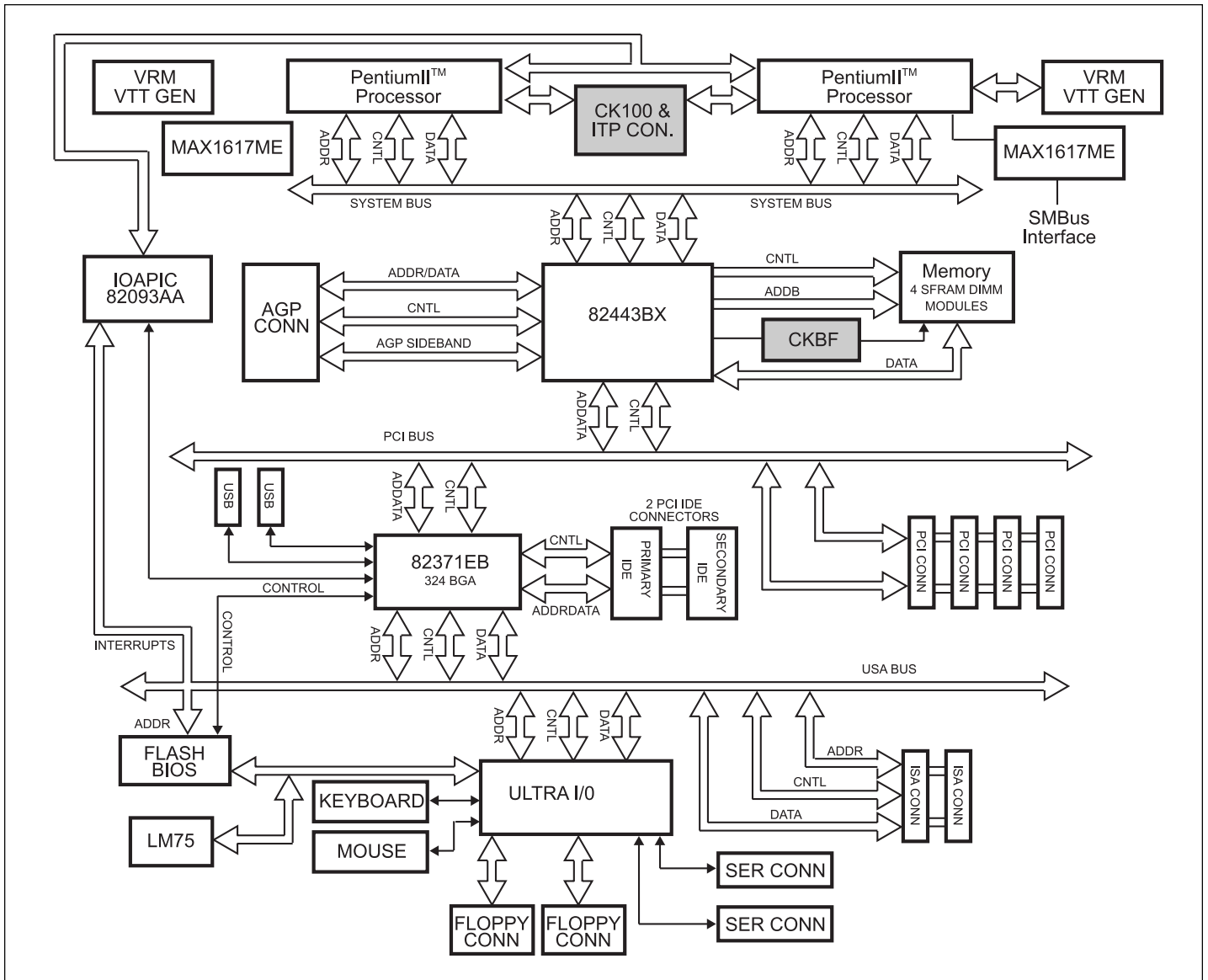


Figure 2. Recommended Layout of a Multiprocessing System

For an efficient system design, effective clock distribution is essential. Developing a synchronous system needs low-skew and low-duty-cycle distortion. System board layouts can significantly reduce cycle budget and margins. Pericom's clock drivers can significantly help reduce design complexities. They provide a skew as low as 250ps at frequencies as high as 100 MHz.

Why Low Skew is Important?

To measure the timing differences between two different clock signal edges, engineers use the term skew. Skew is also the measure of propagation delay between signals that are intended to arrive at various destinations at precisely the same time. The clock signal at a different part of a circuit is used to trigger following stages at the same time so that all elements of the circuitry are synchronized.

With a shorter clock period, such as 10ns at 100 MHz, large skew makes it improbable that a clock signal triggers its load destination. The analysis shows that with a cycle time as low as 10ns, a skew as low as 250ps uses 2.5 percent of the 10ns cycle. This is the uncertainty time measurement for the arrival of a clock signal. The Intel collection of high-performance microprocessors used in personal computers and workstations needs high-quality clock distribution. These clocks are 100 MHz, 66 MHz, 33 MHz, and 24 MHz. They require a symmetrical duty cycle within an error range of 50 ±10% and minimal distribution skew at the leading edge of all clock copies at their destinations of less than 250ps. The clock driver must be able to drive high capacitance loads, i.e., FPGA inputs, plated-through holes for FPGAs, and low Z boards. The problem faced by design engineers are high cost of large multilayer motherboards that precludes termination networks. Termination networks use board real estate and assembly cost.

The microprocessor and controller chip inputs need to swing completely between +0.5V to 3.5V in a low impedance of 50 to 70 ohms of highly capacitate environment. Undershoot and overshoot problems on clock signal because of impedance mismatch, as a result of higher capacitance loads, are also present. Pericom's line of clock drivers, such as PI6C180 and PI6C3818A, are targeted for PC and networking applications respectively. They are perfect examples of clock drivers that can remedy most of the problems mentioned so far. They provide an accurate, jitter-free, and fixed-frequency clocks. These drivers distribute clocks to various components all over the motherboard. To complete a synchronous system, the 250ps skew allows all distributed clocks to arrive at their respective destinations simultaneously. Clocks are undershoot free, close to 50 percent duty cycle.

The variable inductance, capacitance, and length of copper trace, however, may exhibit line impedance anywhere from 50 to 200 ohms. The capacitive loading added to this may distort the original clock duty cycle. Worse, it may even introduce ringing effect. All these problems require good impedance-match termination. Application Brief 23 discusses several methods of line termination. Pericom's drivers provide series source termination within the clock output driver on the device.

Pericom's clock drivers provide an output-to-output skew as low as 250ps. However, when the clock copies originate from the driver, the skew at the clock receptors is result of their wiring length differences. Traces of microstrip lines exhibit an approximate velocity of 150ps/inch. Traces of strip line exhibit a velocity of approximately 200 ps/inch. The clock tree must be carefully designed within an accuracy of 100ps. Daisy chained clock wiring must be avoided, especially with series source termination. When a single fanout connects multiple clock receptors, it is recommended that they be clustered at the end, within two inches of each other. Figure 3 shows a diagram of the clustering method.

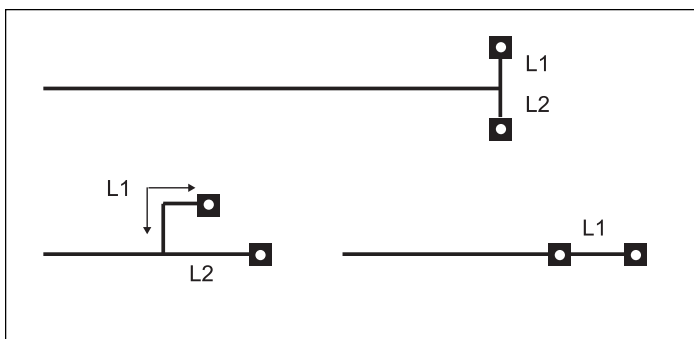


Figure 3. Clustering Method

The input capacitance of these receptors add to each other and result in the lower end of line impedance. A good design also accounts for other capacitance such as large solder-in plated-through holes (5-15pF) and sockets (5-10pF/pin).

PC Board Transmission Line Equations

Shown below we show how to properly calculate line impedance:

Characteristics Impedance

$$Z_0 = \sqrt{L_0/C_0} \text{ (ohms when } L_0 \text{ is in pH/in. and } C_0 \text{ is in pF/in.)}$$

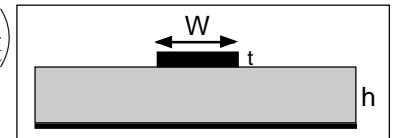
Propagation Delay

$$T_{pd} = \sqrt{L_0 \times C_0} \text{ (ps/in. when } L_0 \text{ is in pH/inch and } C_0 \text{ is in pF/in.)}$$

For Microstrip Topology using G-10 glass epoxy material ($\epsilon_r = 4.7$)

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \times \ln\left(\frac{5.98h}{0.8w + t}\right)$$

$$Z_0 = 35.2 \ln\left(\frac{5.98h}{0.8w + t}\right)$$

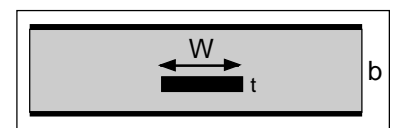


Microstrip

For StripLine Topology using G-10 glass epoxy material ($\epsilon_r = 4.7$)

$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \times \ln\left(\frac{1.9b}{0.8w + t}\right)$$

$$Z_0 = 27.7 \ln\left(\frac{1.96b}{0.8w + t}\right)$$



StripLine

Power On

At power on and the stopping of clocks, clock distribution must show that all clock primary and secondary phases are properly and consistently synchronized. At power up all clock outputs of Pericom's clock drivers are enabled and active.

I²C and Spread Spectrum

I²C control on PI6C18X clock buffers is basically used to control clock lines. To further reduce the EMI emission, I²C control interface allows unused clock outputs to be turned off. During the initial power up, the motherboard BIOS tests the size of the memory. The BIOS determines if a socket has the DIMM RAM module in it. The BIOS then turns off all unloaded clocks with fast edges that could contribute to higher EMI radiation. By turning these clocks off, this reduces Crosstalk and Jitter of the output clocks.

The purpose of the Spread Spectrum EMI reduction techniques is to spread the energy over a frequency range instead of being concentrated on a single frequency. This technique allows the reduction of a peak value of energy and the ability to spread the energy to a level where the energy density is reduced to a thermal noise level. In reality Spread Spectrum technique with Clock ICs allows the clock frequency to be modulated. The amount of modulation determines the amount of EMI reduction. For example for PI6C100, the spread of - 0.5% is the typical modulation figure.

Pericom Clock buffers preserve the integrity of Spread Spectrum clock signals. For a complete discussion of Spread Spectrum, see Pericom Application Note 11.

Summary

We recommend that design engineers identify and measure all clock receptor input capacitance. As discussed, the capacitance of the plated through and also of the sockets must be determined. Highest frequency clock receptors should be tested for tight symmetry and amplitude voltage level specifications. To optimize system performance, designers must carefully consider the attributes of the clock generators and clock buffers. This consideration has been a major challenge for Pericom. Pericom has been focusing on both clock generators and buffers for clock distribution.