

Memory Address Multiplexing Using 3.3V Bus Switch

by Refugio Jones

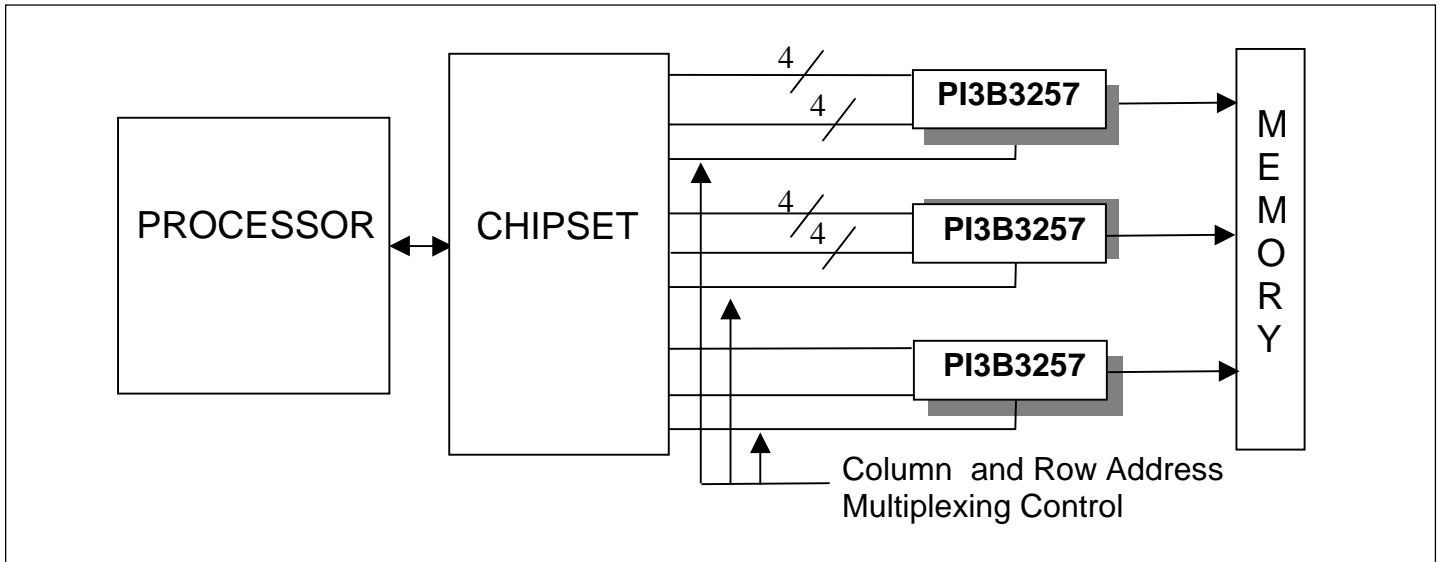
Introduction

Chipsets for popular microprocessors run on 3.3V and interface with 3.3V SDRAMs. In addition, for 100 MHz and greater memory bus applications, the interface timing between chipset and memory is very tight. In these situations, where the row/column address needs to be multiplexed to the memory, Pericom's 3.3V bus switch family is very useful.

An example application using the PI3B3257 3.3V bus switch for column/row address multiplexing is shown below. Here, low propagation delay (0.25 ns) of the 3.3V bus switch and constant on-resistance (5Ω to 10Ω ohms) results in no system penalty with respect to the speed of the system bus.

Application Description

This possible solution accomplishes the task by using Pericom's PI3B3257 3.3V Quad 2 to 1 mux/demux bus switch as shown below. The combined devices multiplex the row and column address to the memory. Control of enabling of row or column address is done by the chipset. The sub nanosecond propagation delay (0.25ns) of the bus switches has little effect on the systems timing and is a clear advantage over other Mux/Demux solutions.



Multiplexing Row/Column Address using PI3B3257 3.3V Bus Switches

