

100 MHz Clock Solution for Desktop Computers

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Introduction

This application brief is the second in a series of documents on PC clock solutions offered by Pericom Semiconductor. This application brief discusses clock generation and clock driver components for use with Intel Pentium II-based PC systems. Pericom's PI6C100 and PI6C104 clock generators generate all the timing requirements as described in Intel's CK97 clock specification. The PI6C100 is designed for dual processor systems, whereas the PI6C104 is designed for single processor systems. The PI6C180 is the companion part to C100, whereas C184 is the companion part of the C104. The PI6C180 and PI6C184 comply with the SDRAM driving requirement specified in the CKBF portion of the CK97 specification. These devices work well within the 100 MHz bus speed specification.

This application brief relates to these Pericom datasheets: PI6C100/104/180/184.

PI6C100/C104

In a Pentium II-based PC system the following clocks need to be generated by the clock generator.

- 2.5V CPU clock
- 3.3V reference clock
- I/O clock
- PCI clock
- 48 MHz clock (USB)
- 24 MHz clock (Super I/O)

PI6C104 is a subset of the PI6C100. The number of outputs for each category of signals is different in the PI6C104 than in the PI6C100.

PI6C100 Functionality & Pin Description

The PI6C100, which comes in 48-pin package, has good distribution of power and ground to reduce and to minimize ground bounce and noise. This device also implements spread spectrum modulation of clock outputs.

Signal Names

REF[0:2] [pin# 1,2,47] These three signals are 3.3V TTL buffered clock output of the xtal frequency. For a PC system this frequency is 14.31818 MHz.

APIC[0:1] [pin#44,45] These output signals, which are used to clock different processors in a dual processor systems are at 2.5V and run at the crystal frequency of 14.31818 MHz.

CPUCLK[0:3] & SEL0, SEL1, SEL100/66#: These four 2.5V CPUCLK output signals are used for different parts of the system, i.e. chipsets and peripherals. The frequency and the output states (Tri-States) are selected by three control pins (SEL0, SEL1, SEL100/60#). Refer to the table below for details.

CPUSTOP# [Pin # 30]: The CPUCLK outputs are forced low when this signal is pulled down low. There is a minimum of two clock synchronizing delays between the CPUSTOP active and the CPUCLK coming to the desired state.

POWERDN# [Pin# 29]: When this signal is active all the clock outputs and the internal oscillators are stopped. The cpu clocks stop at low state.

PCICLK[1:7], PCICLK_F, PCISTOP#: These signals control the PCI clock output of the clock device. PCICLK_F signal is a free running clock. All the other PCI clocks are stoppable by activating the PCISTOP# signal.

PCISTOP# [pin#31] : This signal, when active (low), stops the PCI clock outputs to a low state.

SPREAD#: This is a low active signal. When activated, the clock generator performs spread spectrum modulation of the 100 MHz clock outputs varying it between 99.5 MHz and 100 MHz.

48MHz & 24MHz: These signals are used for USB and Super I/O respectively.

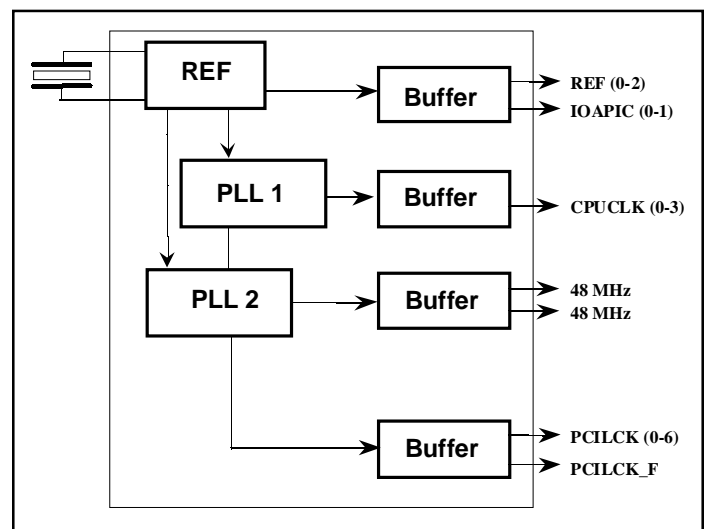


Figure 1. PI6C100 Block Diagram

PI6C104 Functionality & Pin Description

The PI6C104 comes in 28pin package. Signal names and outputs are similar to PI6C100, the number of signals are fewer. This clock generator is designed for single processor applications. The device has good distribution of power and ground to minimize the ground bounce and noise.

Signal Names

REF :These three signals are 3.3V TTL buffered clock outputs of the xtal frequency. For a PC system this frequency is 14.31818 MHz.

APIC: This output signal, used to clock the processor, is a 2.5V signal running at the crystal frequency of 14.31818 MHz.

CPUCLK[0:1] & SEL0, SEL1, SEL100/66#: These four 2.5V CPUCLK output signals are used in different parts of the system, i.e. chipsets and peripherals. The frequency and the output states (Tri-States) are selected by three control pins (SEL0, SEL1, SEL100/66#). Refer to the table below for details.

CPUSTOP [Pin # 30] : When this low active signal is enabled, the CPUCLK outputs are forced low. There is a minimum of a two clock synchronizing delay between the CPUSTOP active and the CPUCLK coming to the desired state.

PCICLK[1:5] : These signals control the PCI clock output of the clock device.

PCICLK_F/S1: This signal is under I²C control. Refer to the selection table in the data sheet for details. The selection is between free running PCI clock and frequency select.

48M/MODE [pin#13] : This dual function pin, whose functionality is programmed by the I²C interface, can function as a 48- MHz output or Mode that determines the power-down condition.

24M/REF/S2 :This is a multiple function pin. The functionality is programmed by the I²C interface. This can function as a 48 MHz

output or “Mode” that determines the power-down condition.

PCICLK [6]: These signals control the PCI clock output of the cl.

48MHz & 24MHz : These signals are used for USB and Super I/O respectively.

Clock Driver : Drives the SDRAM memory systems.

SCLK & DDATA : These are Clock input and serial data input pins to control loading the control bytes for the multiple function pins. Refer to datasheets for details of the bit functions of the bytes.

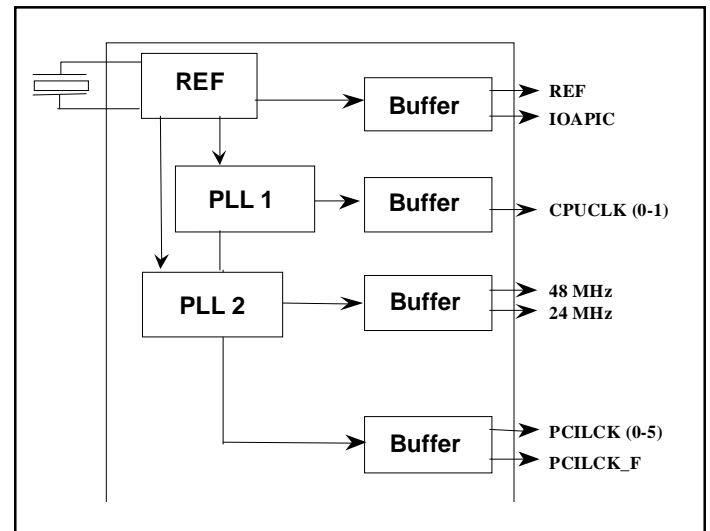


Figure 2. PI6C104 Block Diagram

Table 1. Clock Output Table for PI6C100 and 104

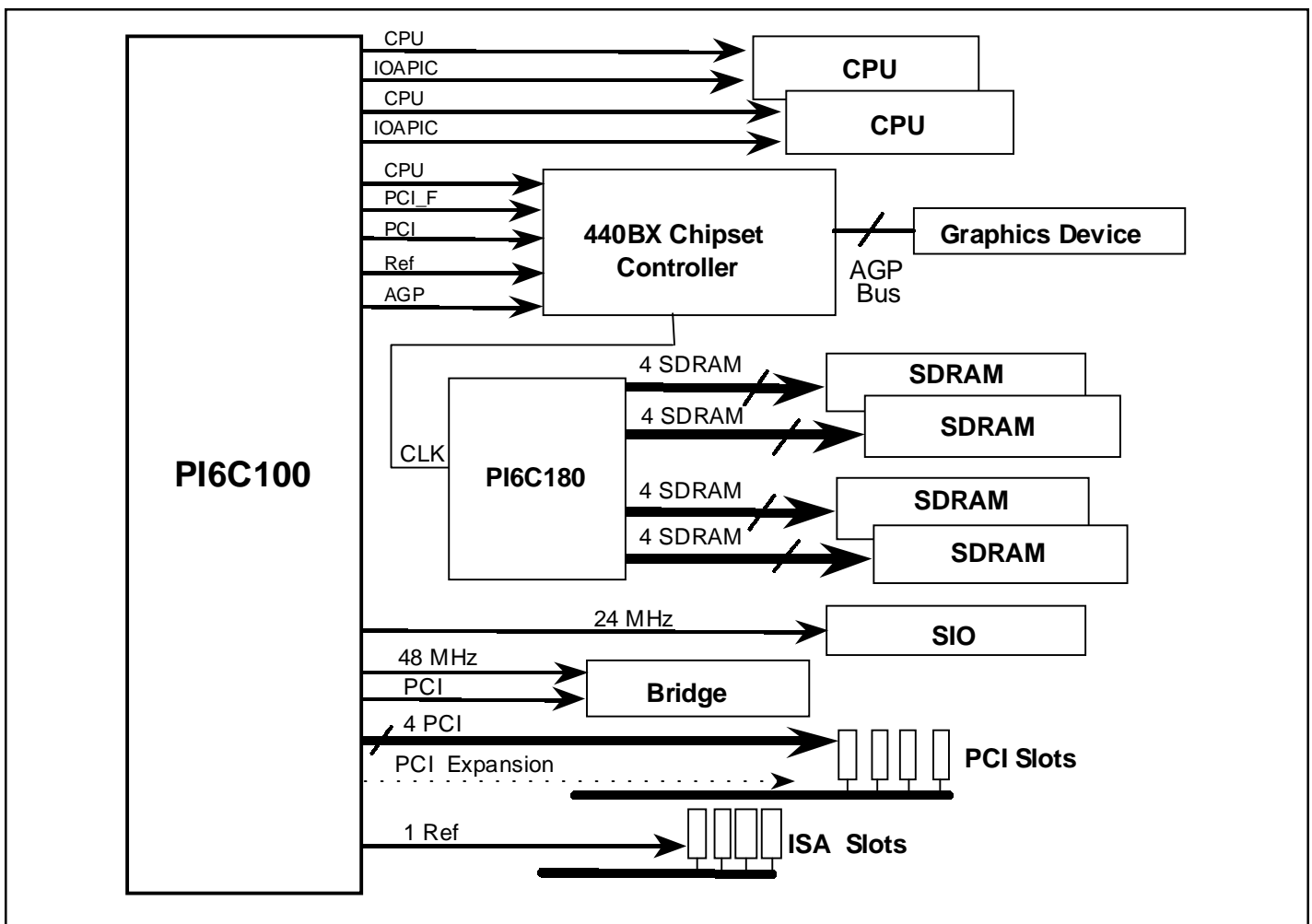
Pericom Part #	Intel Spec.	Number of 2.5V CPUclock	Number of 3.3V Ref. Clock	Number of I/O Clocks (APIC)	Number of PCI Clocks	Number of 48 MHz (USB Clock)	Number of 24 MHz (Super I/O)	Processor/ Chipset	Applications
PI6C100/ PI6C180	CK100 CKBF	4	3	2	8	2		PentiumII/ BX440	Desktop PC or Servers. Supports dual processor. Spread spectrum implemented in the clock generator. Can support 66MHz or 100 MHz. The Clock driver supports 18 SDRAM clocks drivers. I ² C interface to turn on/off the clock drivers.
PI6C104/ PI6C184	CK100 CKBF	2	1	0	7	1	1	PentiumII/ BX chipset	Desktop, single processor PC. Spread spectrum implemented in the clock generator. Can support 66MHz or 100 MHz. The Clock driver supports 18 SDRAM clocks drivers (4 DIMM applications). I ² C interface to turn on/off the clock drivers.

Table 2. Application Summary

	PI6C100	PI6C104
Applications	Desktop	Desktop
No. of CPUs	Dual	Single
Package	SSOP48	SSOP28
FC	No	Yes
SSC	Yes	Yes
48 MHz	Yes	Yes
24 MHz	Yes CK97	Yes

Table 3. PI6C18x Clock Buffer Comparison

	PI6C180	PI6C184
Drivers	18	13
DIMMs	4	3
Package	SSOP48	SSOP28
Applications	Desktop	Desktop


Figure 3. PI6C100 Solution for Server Applications

PI6C180/184 Functionality

These two devices, which are companions to the PI6C100/104, respectively, take the SDRAM Clock outputs from the Bx chipsets and buffers them. The PI6C180 has one input and 18 buffered

outputs, whereas the PI6C184 has one input and 13 outputs. The outputs of the PI6C180/184 are used to clock the SDRAM modules. The PI6C180 can drive 4 DIMMs while the PI6C184 can drive 3 DIMMs.

