

Pericom Offers Solution for PC100 Compliant Modules

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Pericom Semiconductor Corporation introduces its high performance Zero-Delay clock buffers (PI6C2509A and PI6C2910A) that allow zero phase and frequency clock distribution for the PC100. This is the same as PC SDRAM Registered DIMM Specification with PC bus speeds of up to 100MHz. PC100 allows data transfer between processor and memory module DIMMs at a higher rate (100MHz) which enhances the performance and capability of the PC. The PI6C2509A synchronizes all the clocks on both the 168-pin and the 200-pin registered SDRAM memory modules with zero propagation delay. Now available in a 24-pin TSSOP, the PI6C2509A supports spread spectrum modulation of timing signals. It operates faster and consumes less space than alternative devices providing significant improvement in performance and cost. The PI6C2509A/2510A provide the lowest phase error over all frequencies and introduce no additional jitter as a result of Spread Spectrum modulated input clock signals.

The memory bandwidth of high performance microprocessors is increasing at a rapid rate. The future memory bandwidth requirements are also expected to increase as rapidly. High-speed multiple DRAM chips require high speed with low skew clock distribution devices using PLL technology. To meet this need, Pericom has developed a Zero-Delay Clock Buffer that pushes the clock speed to more than 100 MHz. Leveraging Pericom's advanced PLL technology, the PI6C2509A and PI6C2510A are dual bank, general-purpose Zero-Delay buffers providing multiple copies of a single input clock for SDRAM Registered DIMMs. These buffers

fan out of one clock to multiple output in a banked mode. An external feedback pin synchronizes the outputs to the clock input, and series termination. It also operates at 3.3V with no external RC Network.

Both the PI6C2509A and the PI6C2510A have many modes of operation that aid the designer in reducing power consumption, minimizing EMI, and troubleshooting. By disabling a bank, the output clock is pulled down to a low state. The enable/disable feature provides a method of disabling all or part of the clock output without requiring PLL restoration. This feature allows preservation of signal integrity and reduces power consumption and radiated emissions. Additionally, the PLL can be disabled to place the chip in a bypass test mode. In this mode, the input clock is buffered directly to the output and the output buffer only delays the output clock. Jitter characteristics and phase differences created by the PLL can also be analyzed by enabling and disabling the PLL and comparing the characteristics. To have the clock edge arrive at the loads at the same time the clock arrives at the clock buffer input, these buffers can generate a leading clock. This is achieved by matching the propagation delay of the feedback line with the propagation delay of output to load.

Pericom is a leading provider of advanced interface solutions for personal computers including : Bus Switches, Analog Switches, and FCT Logic. As PC performance continues to increase to 400 MHz and beyond, high-performance clocks are essential to sustaining high system performance. Pericom clock technology provides new levels of performance available in PC clock systems.

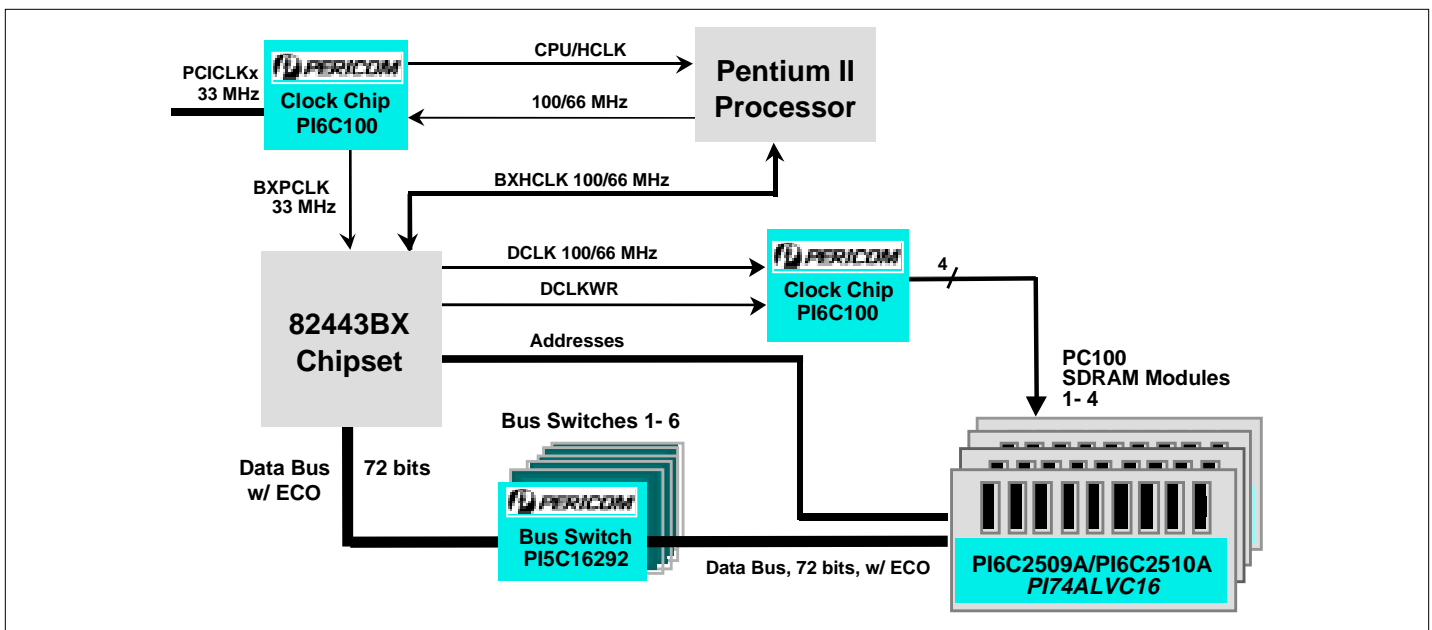


Figure 1. Pericom's Complete PC-100 Interface Solution

Complete solution with Bus Switches and Logic

At 100 MHz bus frequency, the PC100 SDRAM memory module is fast becoming a prevalent memory module. Pericom's ALVC series of logic circuits are state-of-the-art 0.5-micron CMOS technology, achieving industry-leading speed. The PI74ALVC16835, one of the widely used 18-bit registered universal bus drivers, is well balanced, well controlled, and much quieter with a 4ns propagation delay into 100pF of loading. In addition, the PI74ALVC162835 has a built-in 25-ohm series resistor to reduce noise resulting from reflection, thus eliminating the need for an external series termination. Since there

are more than eight SDRAMs on the module, input capacitance for address and control lines is in the order of several hundred-pico Farads - very high for the system. Hence buffers are needed to prevent overloading of the system.

Figure 2 depicts the basic PC100 SDRAM memory module using 64Mbits and 128Mbits memory. The PI6C2509A/2510A clock drivers are needed when you have more than four SDRAM chips to be clocked. A JEDEC standard memory module can have one, two, or four banks, depending on module density and memory chip configuration.

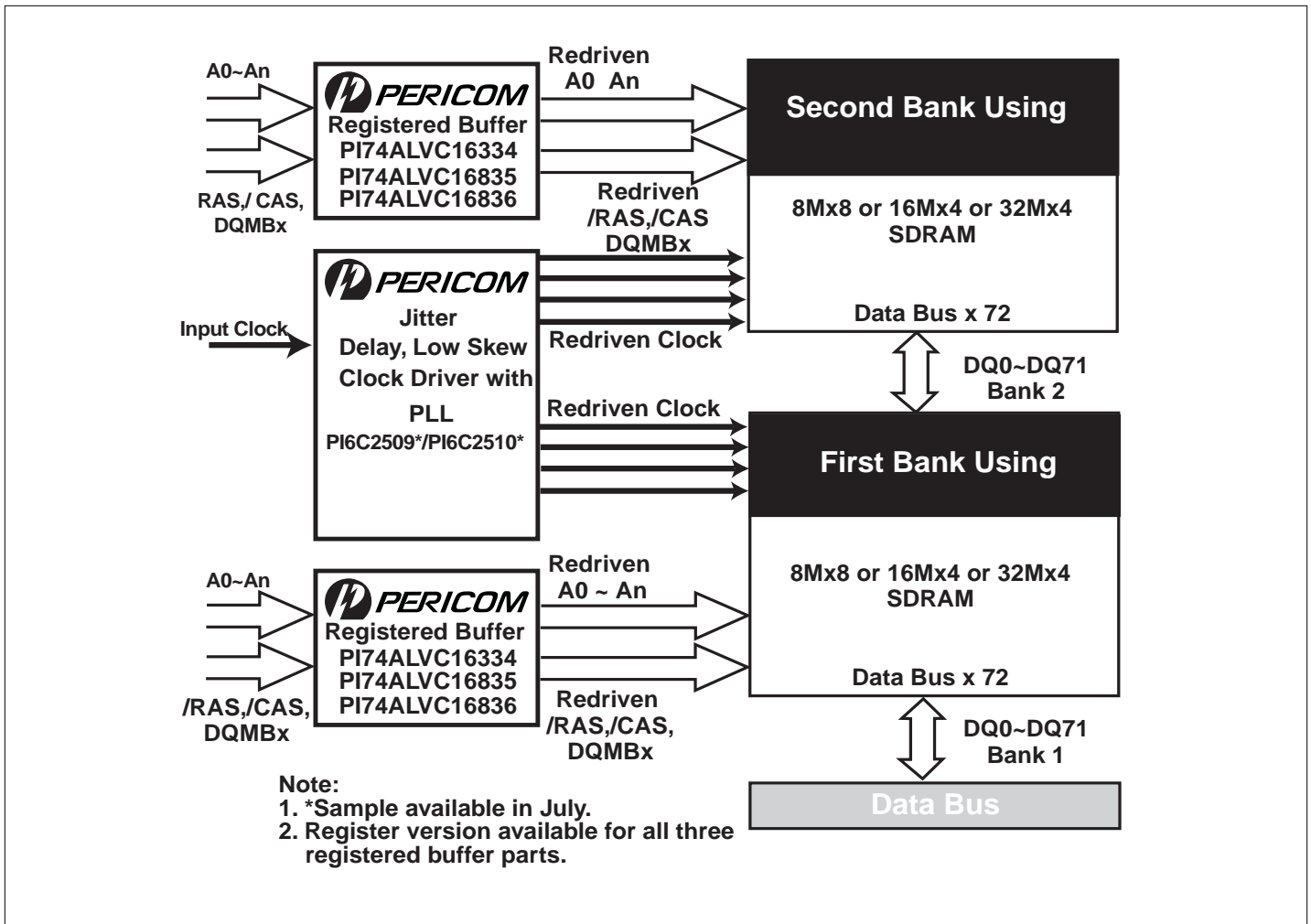


Figure 2. Basic PC100 SDRAM Memory Module

Table 1 shows the x72 SDRAM memory module configuration using 64Mbit and 128Mbit memory chips. Pericom offers registered buffers with and without resistor from 16 bits to 20 bits. The PI74ALVC16334 is a 16-bit-registered buffer, the PI74ALVC16835 is a 18-bit registered buffer, and the PI74ALVC16836 is 20-bit registered buffer. The resistor-registered

buffers are the PI74ALVC162334, the PI74ALVC162835, and the PI74ALVC162836. Tables 2 and 3 recommend which and how many registered buffers and clock drivers to use on which DIMMs. For detailed product information, call our technical support at 800-435-2336 or refer to Pericom's web site at www.pericom.com

Table 1. SDRAM Memory Module x72 Configuration

Module Density	Module Configuration	SDRAM Organization	No of SDRAM	No. of Banks	Pericom's Clock Driver	Pericom's Registered Buffer
64MB	8Mx72	8Mx8	9	1	PI6C2509A PI6C2510A	PI74ALVC16334 PI74ALVC16835 PI74ALVC16233 PI74ALVC162835
128MB	16Mx72	16Mx4	18	1	PI6C2509A PI6C2510A	PI74ALVC16334 PI74ALVC16835 PI74ALVC162334 PI74ALVC162835
256MB	32Mx72	16Mx4	36	2	PI6C2509A PI6C2510A	PI74ALVC16334 PI74ALVC16835 PI74ALVC16836 PI74ALVC162334 PI74ALVC162835 PI74ALVC162836
512MB	64Mx72	32Mx4	36	2	PI6C2509A PI6C2510A	PI74ALVC16334 PI74ALVC16835 PI74ALVC16836 PI74ALVC16233 PI74ALVC16283 PI74ALVC162836

Table 2. Number of registered and clock drivers used for the 64MB/128MB DIMMs

256MB/512MB SDRAM DIMMs			
Two PI74ALVC16334s	Two PI74ALVC162334s	Three PI74ALVC162335s	Three PI74ALVC162335s
One PI6C2509A or one PI6C2510A	One PI6C2509A or one PI6C2510A	One PI6C2509A or one PI6C2510A	One PI6C2509A or one PI6C2510A

Table 3. Number of registered and clock drivers used for the 256/512MB DIMMs

256MB/512MB SDRAM DIMMs			
Two PI74ALVC16334s and one PI74ALVC16836	Two PI74ALVC16334s and one PI74ALVC16836	Three PI74ALVC16835s or three PI74ALVC162835s	Three PI74ALVC16386s or three PI74ALVC162386s
One PI6C2509As or one PI6C2510A	One PI6C2509A or one PI6C2510A	One PI6C2509A or one PI6C2510A	One PI6C2509A or one PI6C2510A

