

Mixed Voltage Memory Module Using PI5C16861 Bus Switch As A Translator

Bus Switch Use In 3.3V DRAM Modules

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Introduction

With today's DRAM modules mixing 3.3V memory devices and 5V TTL logic, serious damage to 3.3V DRAM can occur if inputs are >3.8V (assuming DRAM is not 5V Tolerant). With chip sets and DRAM Controller chips at 5V and new DRAMs at 3.3V, the requirement for level translation is mandatory. This brief will describe how to protect 3.3V DRAM in a 72-pin SIMM module by using the PI5C16861 as a 5V to 3.3V translator.

Circuit Description

The circuit shown below uses three PI5C16861 bus switches. IC1 is used to perform level translation on all control and addressing lines while IC2 and IC3 are used to translate 36 bits of data. All three switches are always enabled because they are used strictly as translators. Notice that if live insertion is required, the bus switch can double as bus isolation. In such a situation, enable pins should be held high with a pullup resistor during insertion.

The 20-bit wide PI5C16861 bus switch is a "straight through" switch with inputs on one side and outputs on the opposite side of the package. This makes layout easier on the PCB module. To make this device into a translator, V_{CC} must be lowered to 4.3V because the basic bus switch is a NMOS device with the substrate connected to ground thus allowing bidirectional data flow through the channel. The 5V V_{CC} is dropped to 4.3V through a signal diode (1N4001 or equivalent) biased with a 2k Ω resistor which is needed to maintain a constant drop at the diode. The 3.3V bus voltage is established because the NMOS bus switch requires a gate-to-source voltage of 1V to conduct ($V_{Th} = +1V$). Thus, to write data to DRAM, a 5V input is translated to a 3.3V input. Conversely, the 3.3V readout data from the 3.3V DRAM is transferred back through the switch to the 5V bus; this is required for bidirectional data flow on the data bus. RAS, CAS, and R/W controls are single directional as are the address bits.

A typical 72-pin SIMM needs the following lines translated:

- 36 - Data I/O bits
- 4 - Column Address Strobe (CAS) bits
- 4 - Row Address Strobe (RAS) bits
- 10 - Address bits
- 1 - Read/Write (R/W) (write active low) bit

For more information please refer to Pericom Application Note 1. Depending on bus width, Pericom also has other bus switches that can be used for this application.



