White Paper

PERICOM®

by Bill Weir (Snr Director Marketing)

Overcoming Advanced Signaling Integrity Issues in High-Speed Systems

INTRODUCTION

As signaling rates continue to increase, maintaining signal integrity has become a much greater challenge for developers. Migrating a system to a next-generation interface operating at 5, 8, 10, or 12 Gbps brings with it increased sensitivity to attenuation and jitter that can severely curtail reach and reliability. Developers must also take into account the impact process technology migration has on output signal drive. For small format platforms like cell phones and other consumer electronics devices that use highly integrated, ultra-low power SoCs, addressing signaling integrity through careful design is even more critical.

Traditionally, efforts to maintain signal integrity have focused on minimizing losses across the communication channel between the transmitter and receiver. However, as the signaling frequency increases, so do the losses across PCB traces, connectors, vias, and cables (see Figure1). High speed signals are also more susceptible to environmental noise. Depending upon the particular protocol in use, at some point the combined losses can exceed the ability of the controller to reliability transfer data (i.e., maintain a bit error rate (BER) of at least 10-12).

A conservative but useful 'rule of thumb' when sizing up channel loss for 'typical' FR4 PCB material is: 'approximately 1dB/inch@10Gbps data rates'. Connector and via losses need to be added on top of that as well.

For developers of systems utilizing high speed interfaces, two new factors are beginning to have a substantial impact on signal integrity: power and process geometry. Today's system-on-chips (SoC) are complex devices that combine processor, I/O, memory, and other functionality on a single chip. To achieve both improved processing

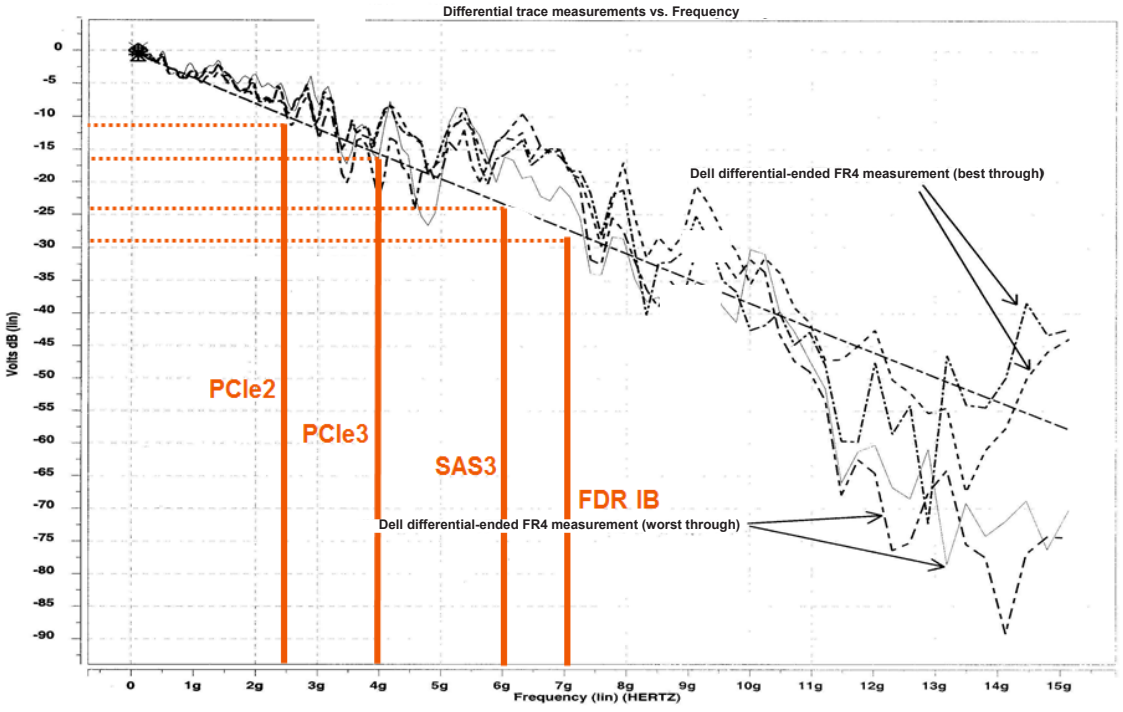

Figure 1: Insertion loss for FR4 material increases with frequency, shown here at 60 cm (24 in). When connector attenuation is included, losses can easily exceed chipset or endpoint maximum drive capabilities, causing the BER to drop below acceptable limits.

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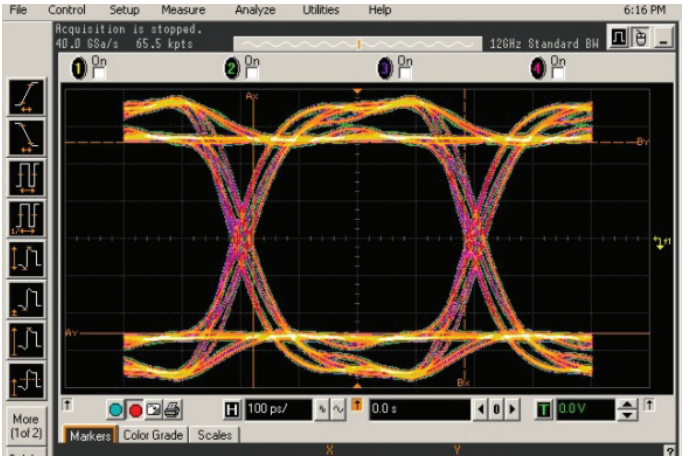

Figure 2: A) At the transmitter, a signal's "eye" is wide open, showing that signal jitter and attenuation are within acceptable limits.

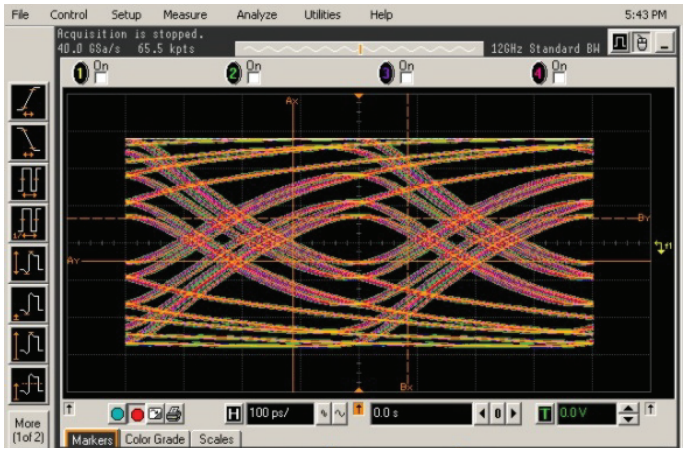

Figure 2:B) Losses from traces, vias, cables, and connectors close the signal eye as it approaches the receiver, increasing the BER substantially and reducing both the reliability and effective throughput of the channel.

performance and greater power efficiency, these SoCs are being designed using smaller geometries operating at lower voltages. Often these devices are designed to be pin-compatible with previous generations to simplify integration into existing designs. Thus, designers can leverage better performance and power consumption often at a lower price as well.

The potential downside of shrinking process geometries is that a SoC's drive signal may be reduced. Consider the challenge facing silicon manufacturers designing chipsets for cell phones and other small form factor systems.

Because these devices are battery-powered, there is tremendous pressure to provide greater performance within the same power footprint so as not to negatively impact battery life. Operating at higher frequencies, however, increases power consumption. Processors maintain a neutral power impact by lowering the operating voltage. Communication channels, on the other hand, have a set output voltage. However, the overall design of a SoC, with all of its different functional blocks architected for ultra-low power consumption, may limit the available drive power and greatly reduce the drive output, and thus drive length, of high speed links. For some SoCs, it just isn't possible to design for ultra-low power and still maintain high drive output.

The effects of today's reduced process geometries on signal integrity can be seen at signaling rates as low as 5 Gbps.

These include lower voltage operation, EMI, and trace/cable length. For example, the drive length of an integrated USB controller may be reduced by half when a SoC is migrated to the next process geometry. Thus, while the SoC is pin-compatible with previous generations, it may not be drive-compatible. Channel losses may become too great for the reduced drive of the signal with the result that communication channels designed within spec using previous generation SoCs may become unreliable when migrated to next-generation devices.

Note that output drive is an issue in more than just portable or other small form factor applications. Power dissipation, for example, is a critical care-about for server equipment and these same factors may impact designs

Restoring Signal Integrity with Signal Conditioning

To verify that devices with high speed interfaces will pass compliance testing, many developers test signal integrity by measuring the signal "eye" at the receiver. Figure 2A shows a signal at the transmitter with its "eye" wide open and that signal jitter and attenuation are within acceptable limits.

Figure 2B shows the same signal at the receiver. With enough signal loss from traces (approx. 1.2 dB/inch for "standard" FR4 PCB at 12 Gbps), vias (up to 2 dB each), cables (1.9 to 4.4 dB/m, depending upon cable quality), and connectors (0.5 to 1.5dB) across the channel, the eye closes and the BER) rises substantially, reducing the reliability and throughput of the channel. Signal conditioning provides a means to restore signal integrity using emphasis and equalization techniques to adjust for jitter and attenuation losses. Somewhere along the communication channel, a device such as a ReDriver or repeater is placed in-line. The ReDriver receives the signal, adjusts for losses that have already occurred, and compensates for losses that will occur along the rest of the channel. Figure 3 shows the signal at the receiver when a ReDriver is used to condition the signal. Opening a closed signal eye restores the signal and the integrity of the data it carries.

Effectively, a ReDriver divides the channel and restores signal integrity at each leg. The result is that the signal can travel reliably over longer distances and additional connectors.

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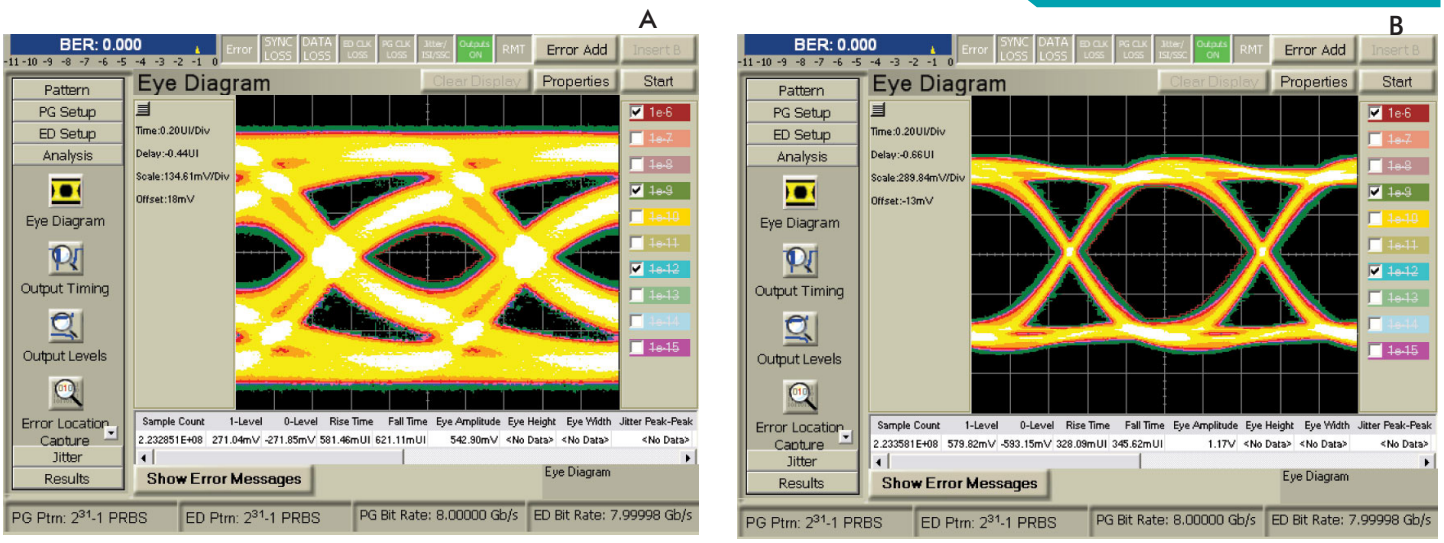

Figure 3: A redriver positioned within the communication channel uses signal conditioning to restore signal integrity by adjusting for jitter and attenuation losses. This opens the signal eye at the receiver, creating a robust interface with high reliability and maximum throughput, as can be seen by viewing a signal A) before and B) after conditioning by a redriver.

To achieve the best performance, the ideal placement for a ReDriver in the channel is the midpoint based on channel losses to divide losses evenly on either side of the ReDriver. For example, if channel loss is 30 dB, it is better for the ReDriver to receive the signal with 15 dB loss and have to compensate for 15 dB loss on the other side than it is for the ReDriver to attempt to overcome 30 dB on one side alone.

ReDrivers provide signal conditioning transparently to the communication channel. They do not decode data or evaluate protocol commands but rather restore the integrity of the original signal and pass it through. ReDrivers also act autonomously; a ReDriver's parameters are chosen based on the channel's characterization and the ReDriver operates independently of the rest of the system.

For applications using cables, as is the case with many consumer electronics applications, signal integrity is especially important. Consumers have expectations about how they expect to use their devices. Consider when a user wants to connect a handset to a TV via a cable. The cable needs to be at least two meters to be able to reach behind the TV and not force the user to stand uncomfortably close to the screen. Note that consumers typically don't reference interface specs; rather, they buy the cable they want and expect it to work. As a result, they may purchase a cable that is longer than specified for the system or use a cable that is of inferior quality and shielding.

The need to support longer and less expensive cables will continue to grow in importance as new applications for portable devices arise. Consider that while these applications may eventually be supported by a wireless link, many are not today. For example, while the majority of consumers have portable devices capable of streaming video, only a limited number of TVs have a wireless connection. Thus, the ability to maintain signal integrity over cables will continue to be an important feature to consumers. "Active" cables using ReDrivers to extend length are now growing in the market.

Optimizing Signal Integrity

To achieve the best performance, the ReDriver needs to have both its input and output characterized to match the actual channel in which it is to be placed. Ideally, high speed interfaces should be designed as a closed channel or restricted open channel, meaning the channel length is fixed with variation in channel loss less than 4 dB. Note that an application with a cable can be designed as a closed channel by providing the cable to be used (i.e., such as the standard cable that comes with every iPhone).

Physical placement of the ReDriver needs to take into account the overall architecture of the system. For example, for many small form factor devices, the midpoint of losses might fall in the middle of an attached cable. In these cases, placing the ReDriver as close to the connector as possible provides the best signal conditioning results. A formal channel analysis should be made to determine the optimal placement.

More complex systems may require different placement.

Consider that the PCISIG 3.0 spec for a "long channel" is 20 dB minimum channel loss for PCI Express. In a server application, however, 20 dB does not provide enough signal margin for a PCB with up to a 34" deep profile and multiple connectors, vias, etc. With a ReDriver, the signal path can be extended; for example, an 8 Gb ReDriver can typically extend a

20 dB channel to 32 dB of compensation, thus increasing PCB trace reach by another 12" to 14" or more for FR4 material.

Complicating placement is the need to keep the mid-plane passive so it can be used with multiple generations of blades. Thus, ideal placement of ReDrivers depends upon the total losses across the blades and mid-plane. Depending upon the server, ReDrivers at the blade connectors to the mid-plane trisect the channel and may provide sufficient signal conditioning.

The Challenge of Integrating Signal Conditioning

One of the advantages of SoC architectures is how they integrate much of the functionality required for an application onto a single chip. Clearly there are advantages to this approach, such as reductions in power, form factor, and cost, as well as greater simplicity of design since functional blocks are intimately coupled with each other. However, there can be diminishing returns to the benefits of integration, and this applies to signal drive.

Consider that when a signal has high drive output, this generates electromagnetic interference (EMI) and creates undesirable noise in nearby circuitry. Within the confined area of a SoC, EMI from a high-speed interface can be especially disruptive to a collocated RF subsystem. This not only decreases radio reliability, it can increase power consumption by forcing the radio to use more power to compensate for reduced transmission range.

The impact of EMI on system reliability depends upon the overall design of the system. In a cell phone, for example, radio antennas are placed at the top of the handset.

Since the battery takes up much of the back of the phone, the

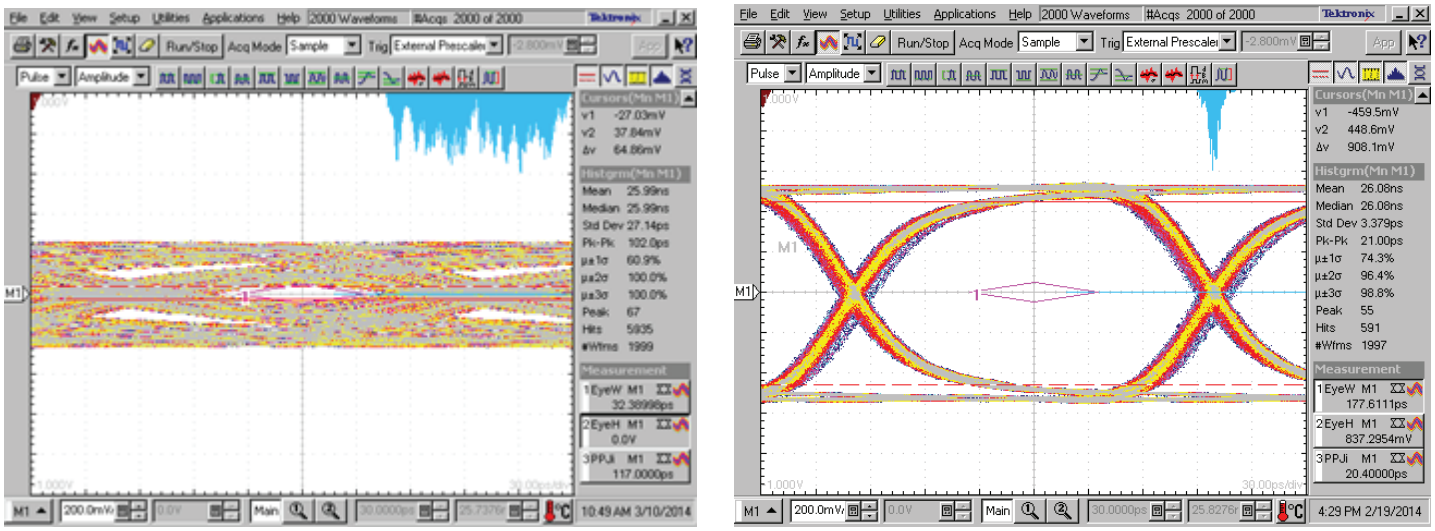

Fig.4A: Left: Input Eye Diagram: Right: Output Eye Diagram; Trace Length=36-in, 5.0Gbps, PRBS7, EQ=Mid

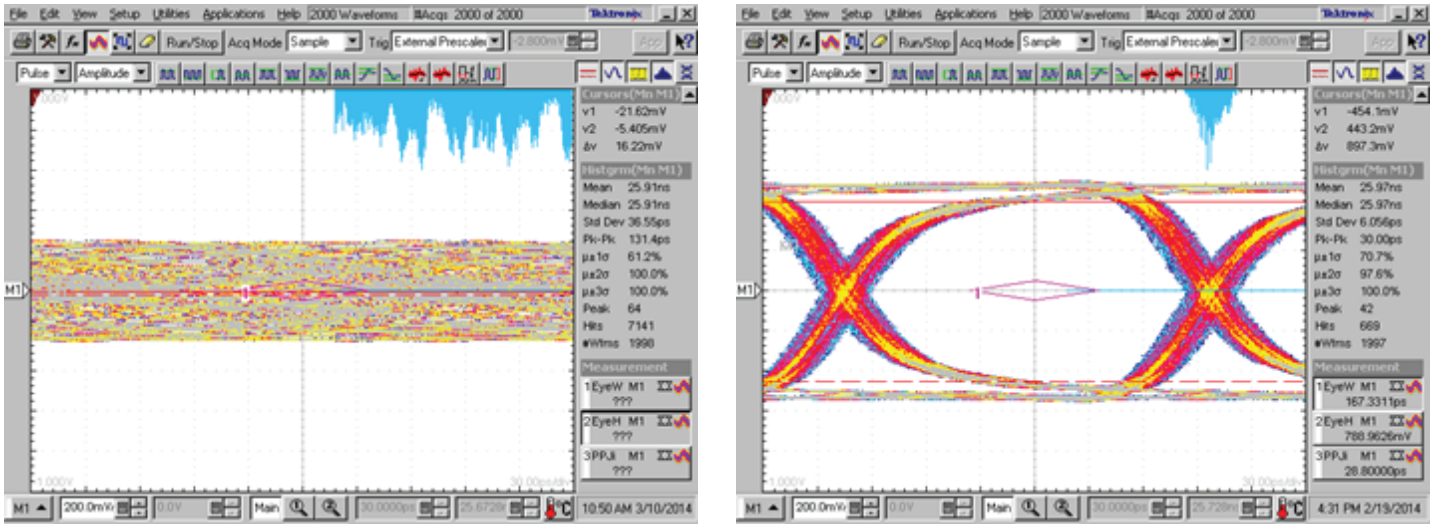

Fig.4B: Left: Input Eye Diagram: Right: Output Eye Diagram; Trace Length=48-in, 5.0Gbps, PRBS7, EQ=High

chip set is located at the top where there is available space as well as to position it near the antennas to reduce trace length and so minimize radio signal losses. To minimize the effect of high-speed communication interfaces on the radio, the connector for these interfaces can be located at the bottom of the handset. If the chip set provides full drive output to the high-speed interfaces, this effectively creates a six-inch antenna through the core of the handset. Not only is the EMI of a large magnitude, it is situated in exactly where it can have the greatest negative impact and cause interference with the entire system. To reduce interference between the RF and USB3 signals, the traces for these interfaces need to be shielded, which can be difficult to achieve given their length, location, and lack of room within the handset's compact form factor.

Another approach is to utilize the SoC's lower drive output to advantage by using an external ReDriver located near the connector. Because the drive current is lower through the handset, this minimizes the EMI transmitted along the signal "spine" between the chip set and connector.

This means less interference and potentially no need for additional shielding beyond what would normally be required for long traces. Because the ReDriver can be situated next to the connector, the signal can be boosted right as it leaves the handset, furthering minimizing any EMI.

In addition, the proximity of the ReDriver and connector makes shielding this portion of the handset much easier and cost-effective. Partitioning the system this way also gives developers greater flexibility in chip set, radio, and antenna placement.

Placing the ReDriver at the edge of the handset also increases the effectiveness of the ReDriver by balancing channel losses on either side of the ReDriver. Consider that when signal conditioning is integrated onto the SoC, the total channel length includes six inches of trace as well as the transition off the chip set. When the signal is boosted and conditioned by a ReDriver close to the connector, any losses between the ReDriver and chip set are handled independently rather than compounded together, providing designers with greater margin to work with. This also maximizes available signal margin to support longer and/or lower quality cables.

The eye diagrams in Figure 4 highlight the USB 3.0 5Gbps ReDriver's ability to open a closed eye, and the drive capability across long channel lengths (source: USB-IF test suite with Pericom PI3EQX7502Ai test card)

Protocol Independence

Another factor impacting signal integrity is link training. Protocols like SAS3, Ethernet KR, and PCI Express Gen3 use an iterative handshake mechanism at progressively higher signaling rates to analyze channel losses between endpoints. This link training process helps the transceiver to determine the best de-emphasis (DE) for the transmitter and equalization (EQ) for the receiver to maximize the eye opening.

This "best fit" is selected from a possible 77 combined Rx EQ and Tx DE settings (for PCI Express Gen3) to determine which achieves the best bit error rate (BER) performance based on maximizing the eye height and width.

The ReDriver itself, however, is not an endpoint and so needs to pass link training signals through without disrupting the training process. Signal conditioning devices that unintelligently condition all signals can interfere with link training and so yield less than optimal performance.

Consider an 8 Gbps PCI Express Gen 3 interface. Gen 3 has numerous presets, some of which use what is called a "preshoot" that emphasizes the leading edge of the waveform. This enables the interface to more clearly delineate between bit transitions and avoid drift issues. However, these preshoots are difficult to track, and a ReDriver with a limiting amplifier that is positioned too close to the controller may clip the preshoot signal during link training. To accommodate this clipping, the ReDriver would have to be moved further from the controller and the channel redesigned to avoid compliance issues.

To eliminate clipping, the ReDriver can utilize a linear amplifier that preserves the input waveform. This preserves the rising edge of the signal and allows the ReDriver to pass all the link training signals through regardless if with preshoot or not. This important feature allows the platform HW designer to take advantage of a ReDriver's inherently lower cost, smaller footprint, and easier PCB routing, compared to other SI solutions.

Signal Conditioning with the Pericom ReDriver/ Repeater Product Families

To help developers meet the tight constraints required for reliable high-speed interfaces, Pericom has introduced two new families of ReDrivers with technology optimized for specific protocols and applications. The PI3EQX89xx/109xx/12xxx family builds upon Pericom's extensive ReDriver portfolio to bring the industry's leading signal conditioning technology to challenging 8 Gbps, 10 Gbps, and 12 Gbps applications. Individual components are available for each of the major signaling standards to provide optimized signal integrity for PCI Express Gen 1, 2, and 3 up to 8 Gbps, 10 Gbps for 10 GbE / 40GbE (10GbEx4) , and 12 Gbps for SAS-3-based systems.

Key features of the PI3EQX family include:

- Support for 4 lanes/8 channels per IC to increase board density and reduce PCB routing issues

Key features of the PI3EQX family (cont..)

- Flow Thru or Interleave pinout options for greater design flexibility
- Advanced analog design in BiCMOS - SiGe process with scalable linear gain to enable further channel and eye adjustments
- I^2C master or slave with up to 16 devices controllable via a single low cost EEPROM
- Low power dissipation of ~1 W at 1V output swing (typ) with all 8 channels active
- Industrial temperature rated for operation from -40 to 85 C
- Single 3.3V power supply
- Industry's smallest TQFN package options

Pericom ReDrivers provide significant advantages for many signal channels over alternative technologies such as Retimers. Retimers improve signal quality and increase signal distance by actually terminating signals and then resending them. This is in contrast to how a ReDriver conditions a signal as it passes the signal through. Retimers are an excellent technology for long open channel interfaces.

However, for the typical channel lengths of most high speed platforms, ReDrivers provide better power consumption (~125 mW/channel), less latency (<0.5 ns), no need for an external clock, and a smaller footprint (TQFN packaging and minimal external R and C components) compared to retimers (see Table 1) for lower overall system cost.

The second new Pericom ReDriver/Repeater family is the latest generation of products optimized for the 5Gbps USB3 protocol standard.

Key features of the USB3 family include:

- Industry's only USB-IF compliant Redriver family
- 1.2V/1.8V/3.3V supply voltages to fit a variety of mobile and fixed platform applications using different CPU/SOC supply voltages
- Fully compliant Power Management modes (U0/U1/U2/U3/more) that monitor and follow host/end point power states to provide maximum battery power savings and industry lowest power consumption.
- Industry smallest packages in 1 channel and 1 port configurations
- I^2C versions for larger platforms such as server, storage, and networking.

Pericom also offers complete families of ReDrivers for DisplayPort, HDMI, SATA 2.0 (3.0Gbps), SATA3.0 (6Gbps), as well as other video ReDrivers with integrated switches (Active Switches).

Pericom supports developers through every step of platform design. To provide the best signal integrity channel matching, Pericom can provide ReDriver IBIS and S parameter models to be used if the customer is doing the channel simulation, or customer can provide S parameters or even physical descriptive models and Pericom can do the channel simulation, working with the customer SI team or hardware design team. The goal is to provide best eye opening and BER settings and initial ReDriver settings. As the design progresses, Pericom can assist with schematic review and then layout review, all which can save substantial development time and money.

Finally, local on-site technical support for system bring up and

	Pericom Redriver/Repeater	Retimer	Redriver/Repeater Advantages
Latency	< 0.5 ns	~500 UI (up to multi uS)	Much lower system latency
Design	PHY level amplifier and EQ	Needs PHY, PCS, PLL — more complex design	Lower unit cost
BOM	Minimal external R and C	More R, C + ref clock circuit	Lower BOM cost Smaller PCB area
Package Options	FlowThru and Interleave Small TQFN package	Large BGA package with Multi-lane neck down.	Smaller PCB area Lower unit cost
Unit Cost	16 lanes (32 ch) = $X / channel in volume	16 lanes (32 ch) = up to $3X / channel in volume	Lower unit cost
Pd	~125 mW / channel	~250 mW /channel	50% lower Pd cost
Channel	Can handle medium length closed channel	Can handle very long open channel	Redriver can work for most channels

Table 1: ReDrivers provide significant advantages over retimers for the typical application utilizing a high speed interface.

debug testing is available worldwide. Developers also have access to evaluation boards, detailed application notes, and expert technical support for all Pericom ReDriver products.

Developers can leverage Pericom's broad experience base to speed compliance design and testing as well. For example, Pericom's PCIe ReDrivers have passed PCISIG Compliance Workshop for Gen2 and Gen3 receiver, transmitter, and interoperability specs. Pericom is also the only IC vendor fully certified by the USB 3.0 Compliance Workshop and listed in the USB-IF USB 3.0 Integrator's list.

Summary

Just as each generation of communication interfaces bring with them greater data rates, so too they introduce new issues for developers to address. The challenge of maintaining signal integrity for high speed interfaces is no longer limited to compensating for the increased sensitivity to jitter and attenuation that comes at higher frequencies. Developers must also account for the lower output drive that corresponds with next-generation SoCs as ICs become more integrated and process geometries continue to shrink, EMI channel effects, and ultra-small platform space and power constraints – with the overall goal of providing the most cost effective solution.

Through the use of robust signal conditioning technology like Pericom's many protocol families of ReDrivers/Repeaters, designers of platforms from large to ultra-small can benefit from the performance, support, and cost effectiveness provided by these products.

References & Links:

Link to AN359: Pericom PCIe ReDriver/Repeater Compatibility in a GEN3 Channel

Link to recent ReDriver articles: Signal Integrity in a GHz World

Pericom Product Links:

ReDriver / Repeater IC Signal Conditioners

PCI Express 1.0 ReDrivers/Repeaters

PCI Express 2.0 ReDrivers/Repeaters

PCI Express 3.0 ReDrivers/Repeaters

USB 3.0 ReDrivers/Repeaters

10GbE ReDriver/Repeater

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