PI2EQX6811ZDE

PI2EQX6811ZDE Evaluation Board Rev.B User Guide

Nov.16, 2011

Contents

Introduction

PI2EQX6811ZDE Evaluation Board is designed to allow convenient testing of its operation and features. This board can work with readily available SATA and eSATA cables for easy connection to SATA3.0 HDD, SSD, OMD storage components and PC system hosts.

This board allows the PI2EQX6811ZDE device to be powered in +1.5V directly from external power, or 5V with a mini-USB connector provided to convert.

This User Guide describes the setup, configuration and operation of PI2EQX6811ZDE Eval Board Rev.B. Figure1 provides a top view of PI2EQX6811ZDE Eval Board Rev.B, and Figure2 is bottom view of the board.

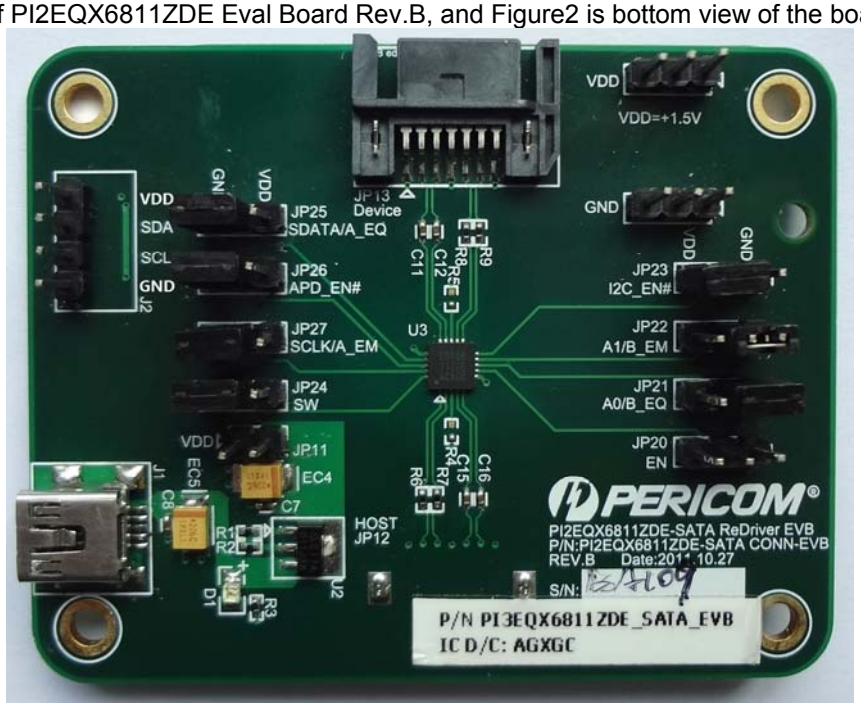


Figure1. Top view of PI2EQX6811ZDE Eval board Rev.A

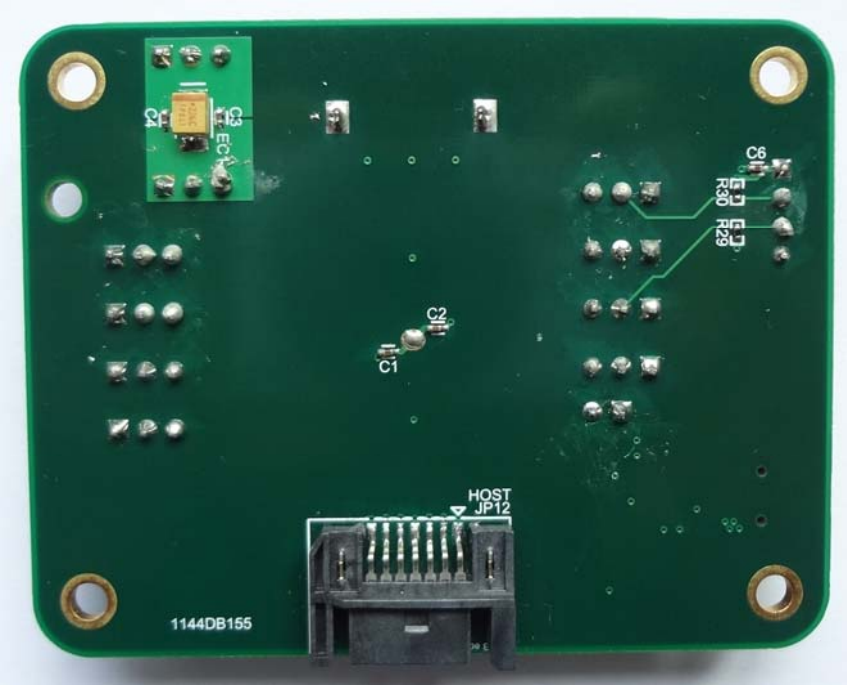


Figure2. Bottom view of PI2EQX6811ZDE Eval board Rev.A

Board Operation

PI2EQX6811ZDE is a 1-port (2-channel), bi-directional, signal SATA3.0 re-driver to provide indication when the load is connected to HOST or Device. Figure3 shows the logical block diagram of PI2EQX6811ZDE. Two channels of the PI2EQX6811ZDE are fully independent in operation and configuration by I2C function. Channel configuration of output pre-emphasis, output swing and input equalization must be set appropriately to match the attached cable/trace length and type.

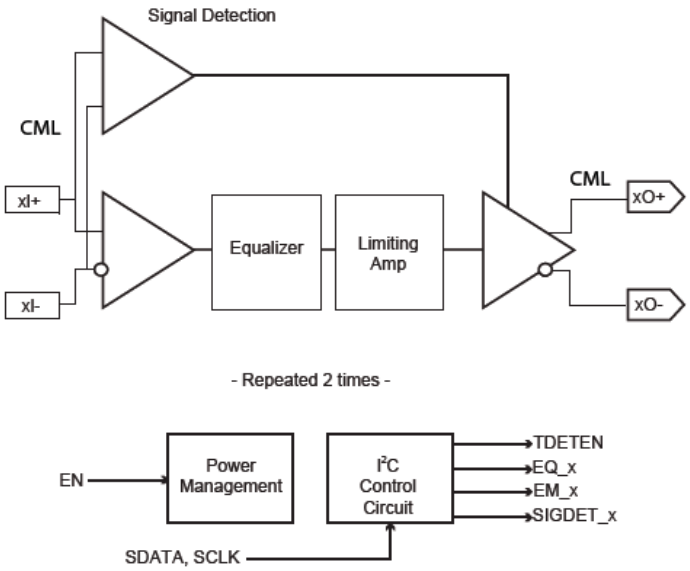


Figure3. Logical Block Diagram of PI2EQX6811ZDE

Power Options

The PI2EQX6811ZDE Evaluation Board provides the options for supplying +1.5V directly or +5V power from mini-USB connector. Figure 4 circles the important connections.

1) Using the +5V power supplied by miniUSB connector (**J1**). The on-board LDO down-steps the voltage to +1.5V. When using this source, note that jumper JP11 must be shorted (populated).

2) Using +1.5V power input directly by **JP18** power pin header and **JP19** ground pin header. When using this method, JP11 must be open.

3) For PI3EQX6801ZDE power supply, the evaluation board is shipped from the default with +1.5V from externally power supply.

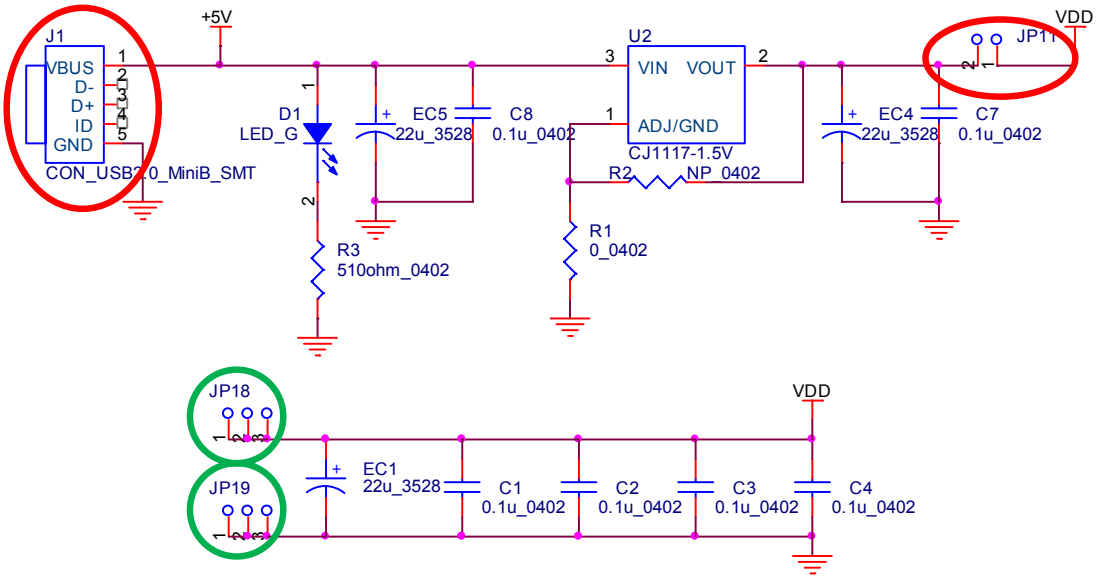


Figure4. Power supply of PI2EQX6811ZDE

Device Configuration

The PI2EQX6811ZDE ReDriver supports Pre-emphasis, swing adjustment and input equalization for optimum operation and signal margins.

PI2EQX6811ZDE provides two ways configuration controls depending on the state of the I2C_EN# pin.

- When I2C_EN# is set to HIGH (JP23 to VDD), the configuration input pins set the configuration operating state and changes to these control pins will change the operating I2C_EN#. For pin configurations, there are some configuration values to be selected only.
- When I2C_EN# pin is set to LOW (JP23 to GND), reprogramming of these control registers via I2C is allowed. For I2C configurations, all the configuration values can be used by I2C as default configuration on EVB.

Table1 shows the pin functions for pin control and I2C control.

<table>
<tr><th>PIN NAME</th><th>PIN Control FUNCTION</th><th>I2C Control Function</th></tr>
<tr><td>P7:EN</td><td>With Internal 100k-ohm pull-up resistor
High: Normal Operation
Low: Power Down Mode</td><td>Same as Pin control function</td></tr>
<tr><td>P8:A0/B_EQ</td><td>Input Equalization for Channel B
Tri-level control
<table><tr><th>JP21</th><th>Input Equalization for Channel B</th></tr><tr><td>GND</td><td>8dB</td></tr><tr><td>Open</td><td>4dB</td></tr><tr><td>VDD</td><td>16dB</td></tr></table></td><td>I2C Programmable address bit A0</td></tr>
<tr><td>P9:A1/B_EM</td><td>Pre-emphasis control for Channel B
Tri-level control
<table><tr><th>JP22</th><th>Input Equalization for Channel B</th></tr><tr><td>GND</td><td>2dB</td></tr><tr><td>Open</td><td>0dB</td></tr><tr><td>VDD</td><td>3.5dB</td></tr></table></td><td>I2C Programmable address bit A1</td></tr>
<tr><td>P10:I2C_EN#</td><td>I2C Enable
High: pin control
Low: I2C control</td><td>Same as Pin control function</td></tr>
<tr><td>P17:
SDATA/A_EQ</td><td>Input Equalization for Channel A
Tri-level control by JP25
Setting Value same as P8</td><td>I2C Data Line</td></tr>
<tr><td>P18:APD_EN#</td><td>Auto stumber mode Enable
High: disable
Low: enable</td><td>Don't Care</td></tr>
<tr><td>P19:
SCLK/A_EM</td><td>Pre-emphasis control for Channel A
Tri-level control by JP27
Setting Value same as P9</td><td>I2C Clock Line</td></tr>
<tr><td>P20:SW</td><td>Output Swing control for Channel A&B
Tri-level control
<table><tr><th>JP24</th><th>Output Swing for Channel A&B
mV(Vtx diff pp) at 3Gb/s</th></tr><tr><td>GND</td><td>667</td></tr><tr><td>Open</td><td>533</td></tr><tr><td>VDD</td><td>900</td></tr></table></td><td>Don't Care</td></tr>
</table>

1) Pin Configurations

Configuration begins with I2C_EN# pin with **JP23**, which must be connected to VDD. The EN pin of the PI2EQX6811ZDE has an internal 200K pull-up resistor to define a high level default (**JP20** Open) for normal operation.

When EN pin is shorted to GND (**JP20** is shorted to GND), device operation is disabled. This is useful for checking PI2EQX6811ZDE disabled-state power consumption. Figure5 is pin strap configuration for pin headers.

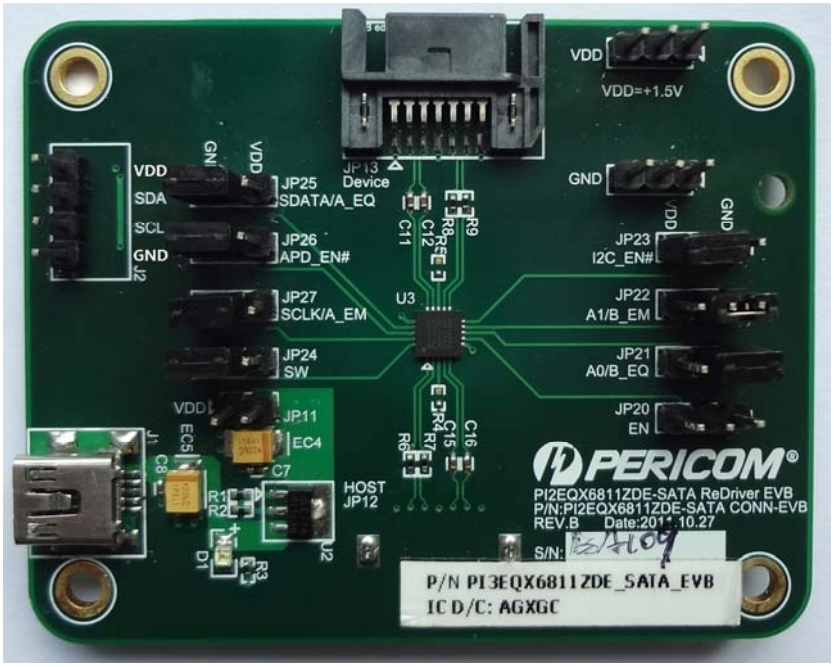


Figure5. Pin Strap Configuration of PI2EQX6811ZDE

◆ **Input Equalizer Setting**

Input equalizer setting has P17 (A_EQ) and P18 (B_EQ) tri-level configuration by JP25 and JP21. So it is available with 3 values in **Blue** color in Table1 below.

◆ **Output Pre-emphasis Setting**

Output Pre-emphasis setting has P19 (A_EM) and P9 (B_EM) tri-level configuration by JP27 and JP22. Table1 shows its selectable setting values.

◆ **Output Swing Setting**

Output Swing setting has P20 (SW) tri-level configuration by JP24. Table1 shows its selectable setting values.

◆ **Auto-slumber Mode Enable Setting**

Auto-slumber mode enable setting has P18 (APD_EN#) configuration by JP26. When JP26 is connected to GND, auto-slumber mode will be enabled, but it is connected to VDD, auto-slumber mode will be disabled.

2) I2C Configuration

On PI2EQX6811ZDE EVB, I2C_EN# pin (**JP23**) is shorted to GND on EVB, I2C configuration is enabled for all the setting as default. And P8 (JP21, A0) and P9 (JP22, A1) pins are also shorted to GND as default I2C address-**C0**. Figure6 is their locations on EVB and I2C interface connector definition and location.

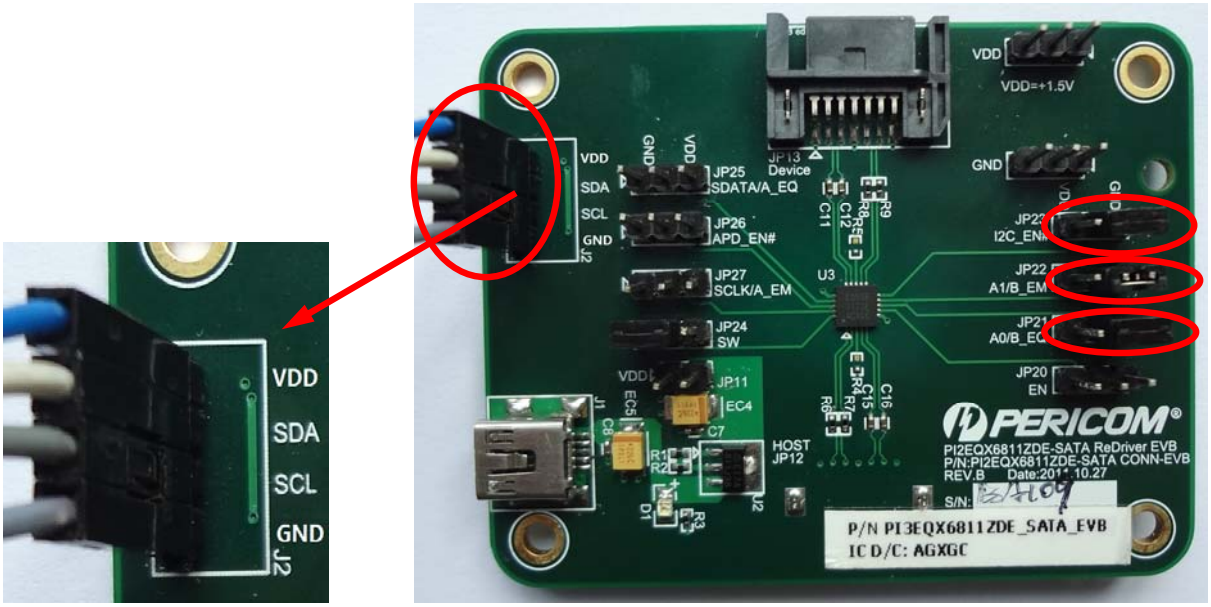


Figure6. I2C address Pins Jumper and Interface location

For PI2EQX6811ZDE's I2C interface, it is compliant with 3.3V power. Figure7 is read/write waveform sample at the register value below for the reference.

Address	R/W	Data
C0	Write	00,14,14,64,B0,C0,90,00,00,00,00,00,00,00,00,00
C1	Read	14,14,64,B0,C0,90,00,00,00,00,00,00,00,00,00

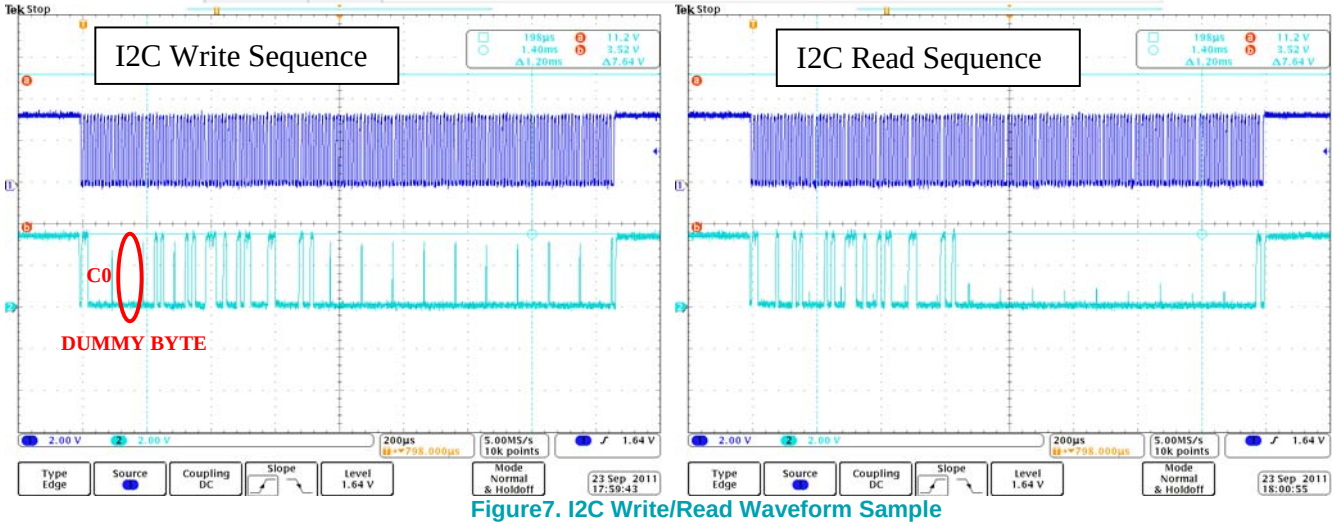


Figure7. I2C Write/Read Waveform Sample

NOTE that there is one dummy byte in Write Sequence.
For detail I2C register description, please refer to **Page7-10** in datasheet.

3) Board Connection

Figure8 is board connections for the reference.

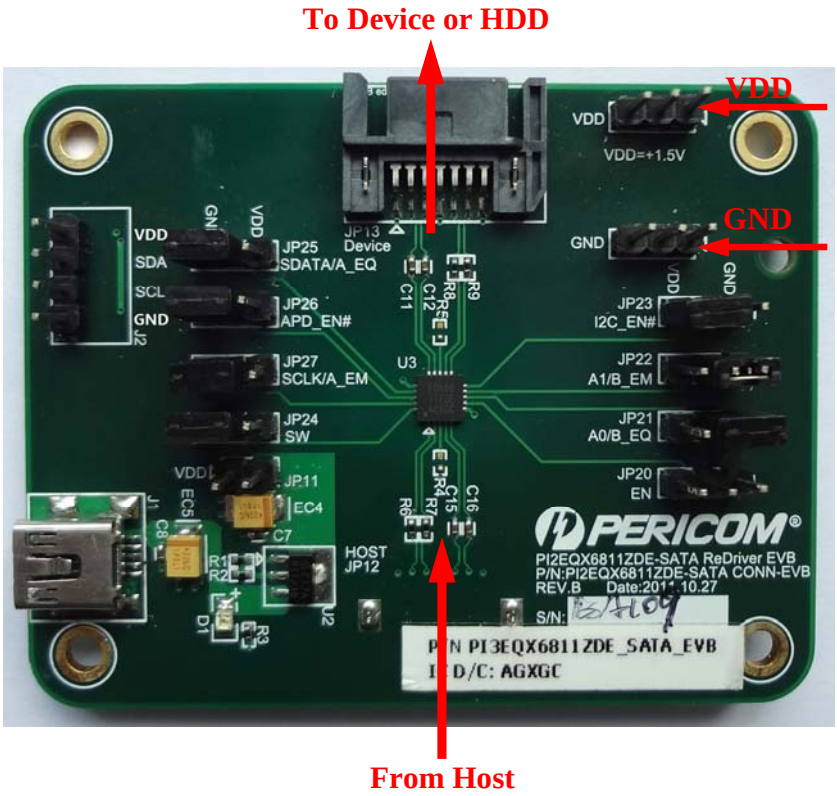


Figure8. Board Connection

- **System Connection**

The diagrams below show some example system test setups with the PI2EQX6811ZDE Eval Board.

Figure9 shows the connection using a NB PC and eSATA Express Card. Note that many notebooks PCs already offer an eSATA port which can be used as the test signal source without the add-in card.

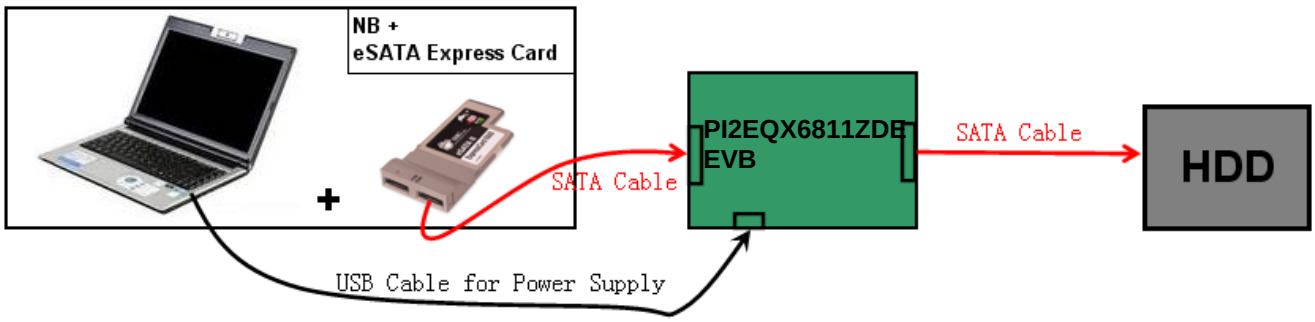


Figure9. eHDD connection Test Setup using NB+eSATA Express Card with PI2EQX6811ZDE Eval Board

Figure10 shows the connection using Intel MB

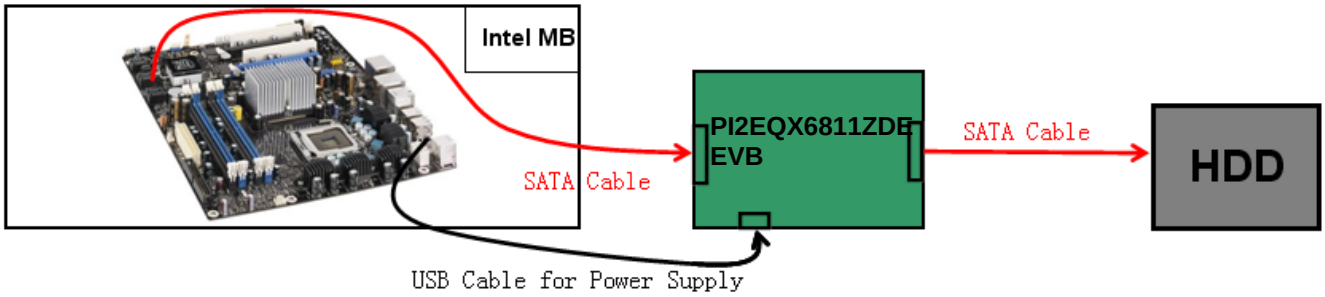


Figure10. internal HDD connection Test Setup using Intel MB with PI2EQX6811ZDE Eval Board

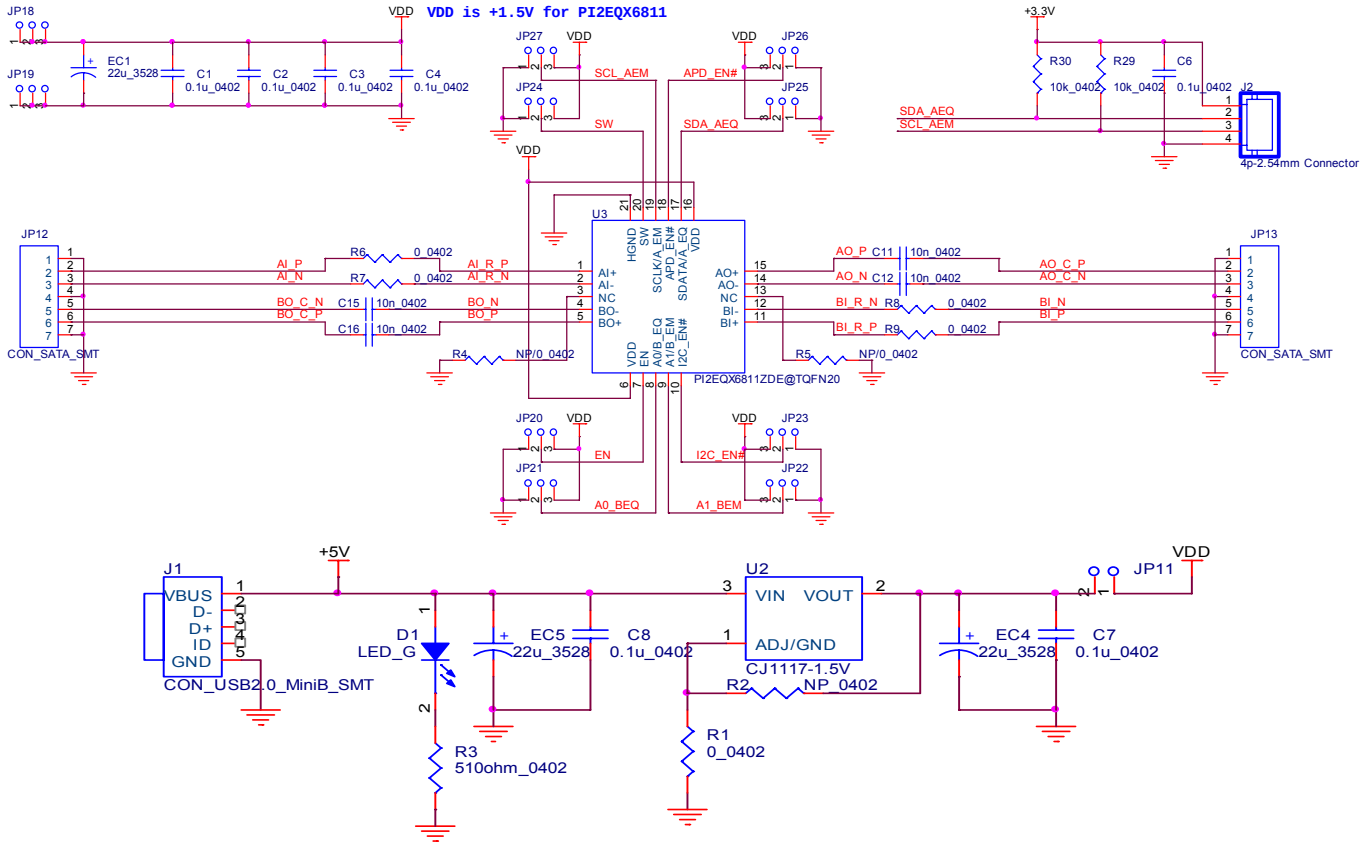
- **Power-on Sequence**

It is recommended as good practice, that all system components be powered off while connections and configuration settings are made. There is no specific power-on sequence required when applying power to the PI2EQX6811ZDE Eval Board. When connected to the system and powered by USB as shown above, then all devices will power-up together.

If the host PC and/or HDD are powered on, while the Eval Board is off, there will be no damage to the PI2EQX6811ZDE under typical conditions. If the Eval Board is then powered on, the system will generally detect the SATA HDD as a hot-plug event, and the HDD will begin to operate properly. Note that some PC systems offer BIOS control over hot plug events, and if the HDD is not recognized, this BIOS setting is the most likely cause and should be changed. When connecting to the system as shown above, all devices will power on together and avoid this BIOS issue.

Board Design Information

- **PCB Schematic**



- **PCB Layout Reference**
  a. Stack Up:

Layer #	Plane	Material type	mil
	Solder Mask		0.4
Layer 1	Signal		1.9
	Prepreg	Prepreg 1080 Prepreg 2116	7.3
Layer 2	Gnd		1.2
	Core		44
Layer 3	Power		1.2
	Prepreg	Prepreg 2116 Prepreg 1080	7.3
Layer 4	Signal		1.9
	Solder Mask		0.4

  b. Isolation Spacing = 30 mil
  c. Width & Spacing (W/S) of 100Ω Differential Trace = 10 / 9 mil

- **PCB BOM List**

Reference	Description	Package	Qty
U2	LM3674-1.5V	SOT23-5	1
U3	PI2EQX6811ZDE@TQFN20	TQFN20	1
Bare PCB	PCB, PI2EQX6811ZDE-SATA ReDriver Rev.B	PCB	1
D1	LED	0805	1
JP12,JP13	SATA L-type connector	L-type	2
J2	4p-2.54mm Connector	2.54mm	1
J1	miniUSB connector	B-type	1
JP11	2PIN HEADER	2.54mm	1
JP18,JP19,JP20,JP21,JP22, JP23,JP24,JP25,JP26,JP27	3PIN HEADER	2.54mm	10
C11,C12,C15,C16	Ceramic Capacitor, 10nF	0402	4
C1,C2,C3,C4,C6,C7,C8	Ceramic Capacitor, 0.1uF	0402	7
EC1,EC4,EC5	Tan cap, 22u	3528	3
R3	Chip Resistor, 510ohm	0402	1
R29,R30	Chip Resistor, 10Kohm	0402	2
R1,R6,R7,R8,R9	Chip Resistor, 0ohm	0402	5

History

Version 1.0	Original Version	Nov 16, 2011