PI2EQX6811ZDE
One-lane SAS/SATA ReDriver Application Note
Nov. 1, 2011

Contents

General Introduction
PI2EQX6811ZDE is a low power, signal SATA Gen3i, SAS2 6.0Gbps ReDriver™. It provides programmable equalization and output pre-emphasis, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference.
PI2EQX6811ZDE provides pin strap and I2C function to set output swing/pre-emphasis and input equalization. It also has termination detect feature when the load is connected to HDD or Host. This can be used as control to go into power saving mode by the device.

Packaging: 20-contact TQFN (4x4mm) for PI2EQX6811ZDE

Main Application:
- ✓ ***Notebook/Docking Station***
- ✓ ***Desktop***
- ✓ ***Storage/Workstation***

Figure1 is typical application sample.

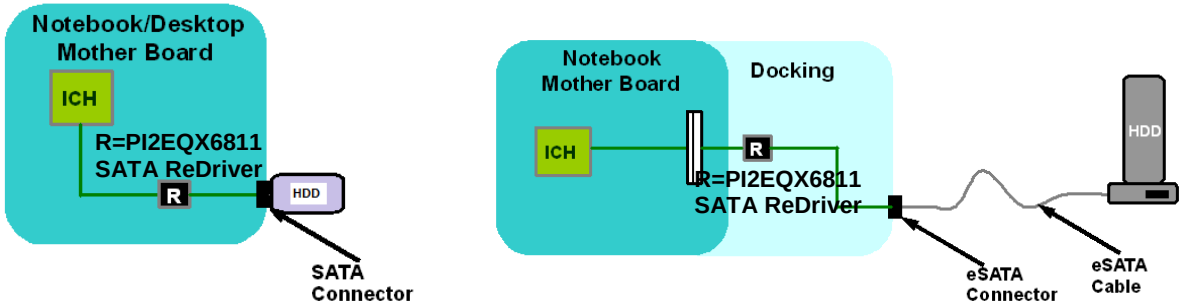


Figure1 Typical Application Sample

How to use pin control and I2C control for output swing/pre-emphasis and input equalization of PI2EQX6811

PI2EQX6811 provides two ways to set output swing/de-emphasis and input equalization.

1, pin control function

2, I2C control function

And they depend on the state of the I2C_EN# pin.

When I2C_EN# pin is set HIGH, all the configuration input pins determine all the configuration settings. Note that EN pin has 200k internal PULL-UP resistor, APD_EN# pin has 200k internal PULL-DOWN resistor, and other pins such as A_EQ/B_EQ, A_EM/B_EM and SW are tri-level control (Low, Open and High). The configuration tables are in Page3 of PI2EQX6811 datasheet.

When I2C_EN# pin is set LOW, all the internal configuration registers can be programmed by I2C function. Note that during initial power-on, the value at the configuration input pins should be referred to Register Description in Page4-6 of PI2EQX6811 datasheet as initial startup states.

- The integrated I2C interfaces operate as a slave device, supporting standard rate operation of 100Kbps, with 7-bit addressing mode and LSB indication either a read or write operation as shown below. The address for a specific device is determined by A0 and A1 pins with internal pull-up resistors. So up to four PI2EQX6811 devices can be connected to a single I2C bus.

Address Assignment							
A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	0	Programmable	Programmable	1=R, 0=W

- Data bytes must be 8-bits long and transferred with MSB first. Please see I2C data transfer diagram in Page8-9 of datasheet. For data byte definition as below, please see Page4-6 of datasheet in detail.

Configuration Register Summary

Byte	Mnemonic	Function
0	A_CNTRL	A_Channel receiver and output control
1	B_CNTRL	B_Channel receiver and output control
2	GBL_FUNC	Global function control
3	A_STATUS	A_Channel status read out
4	B_STATUS	B_Channel statue read out
5-14	Reserved	Reserved registers. Please do not change the value from its power-on state.

**In Byte2, when the compliance test is done, Bit7 should be set to 0 to disable termination detect function.*

- For I2C inputs, SCL and SDA pin are tolerant with +3.3V power.
- For I2C configuration sequence in detail, please see Page6-7 in this file.

External Components Requirement

PI2EQX6811 requires AC coupling capacitors for all redriver outputs. High-quality, low-ESR, X7R, 10nF, 0402-sized capacitors are recommended.

Layout Design Guide

- **Layout Considerations for Differential Pairs**

- ✓ The trace length miss-matching shall be less than 5 mils for the "+" and "–" traces in the same pairs
- ✓ Use wider trace width, with 100ohm differential impedance, to minimize the loss for long routes
- ✓ Target differential Zo of 100ohm ±20%
- ✓ More pair-to-pair spacing for minimal crosstalk coupling, it is recommended to have >3X gap spacing between differential pairs.
- ✓ It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces
- ✓ The use of vias should be avoided if possible, if vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair.
- ✓ Route the differential signals away from other signals and noise sources on the printed circuit board

■ **PCB Layout Trace Routings**

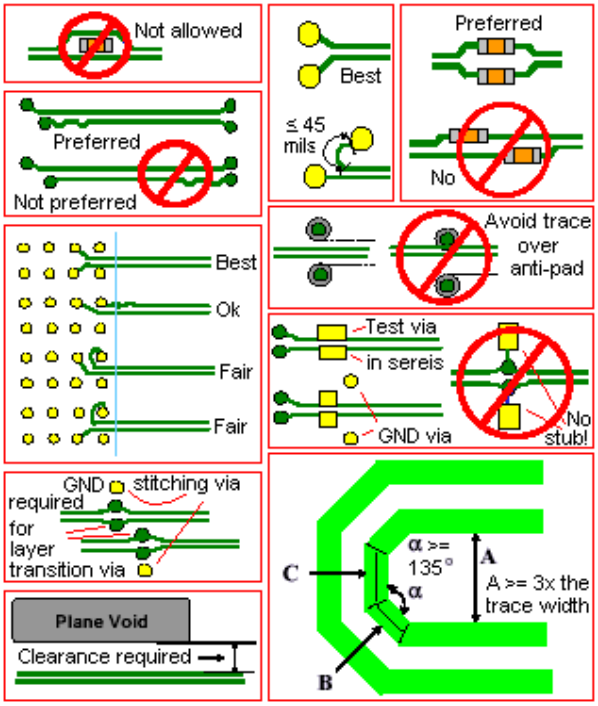


Figure2 Layout Sample for Trace Routings

Power-Supply bypass

More careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply; there are some approaches as recommendation.

- ✓ The supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The distance to plane should be <50mil.
- ✓ The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.
- ✓ Careful attention to supply bypassing through the proper use of bypass capacitors is required. A low-ESR 0.01uF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to PI2EQX6811. Smaller body size capacitors can help facilitate proper component placement. The distance of capacitors to IC body should be <100mil.
- ✓ One capacitor with capacitance in the range of 1uF to 10uF should be incorporated in the power supply bypassing design as well. It is can be either tantalum or an ultra-low ESR ceramic.

Power Supply Sequencing

Proper power supply sequencing is recommened for all devices. Always apply GND and VDD before applying signals., especially if the signal is not current limited.

Caution: Do NOT exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Equalization Setting

- **Various Input Trace and Eye Test with different EQ setting**

Figure3 is PI2EQX6811 test setup for different EQ setting, R is PI2EQX6811.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, Pre-emphasis is 0dB

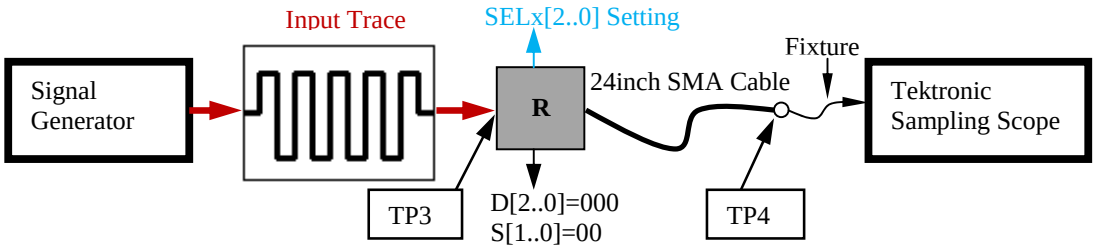
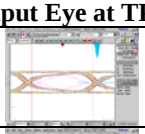
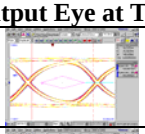
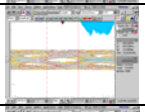
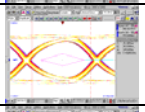
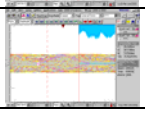
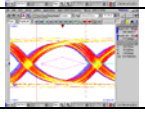


Figure3 PI2EQX6811 test setup for different equalization setting

Table1 Eye Diagram at TP4 vs. Input FR4 trace and EQ setting at 6Gb/s for PI2EQX6811

	Input Trace Length	SEL[2..0] Setting	Input Eye at TP3	Output Eye at TP4
Eye Diagram vs. EQ setting at 6Gb/s	6 inch FR4 Lab trace (-2dB loss at 6GHz)	8dB (SEL[2,1,0] =010)		
	30 inch FR4 Lab trace (-10dB at 3GHz)	12dB (SEL[2,1,0] =110)		
	48 inch FR4 Lab trace (-16dB at 3GHz)	16dB (SEL[2,1,0] =111)		

Output Swing Setting

Figure4 is PI2EQX6811 test setup for different output swing setting, R is PI2EQX6811.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, Pre-emphasis is 0dB

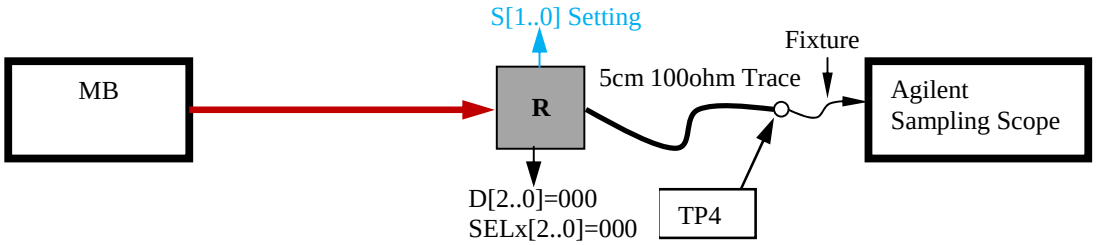
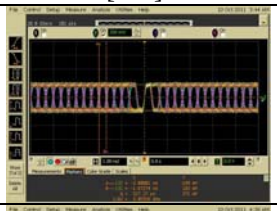
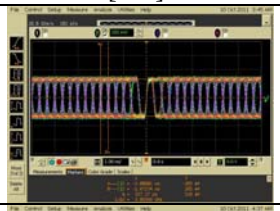
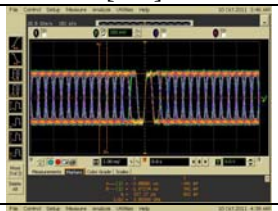
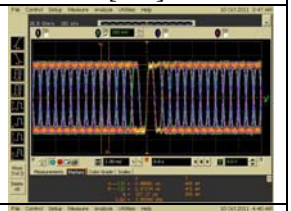
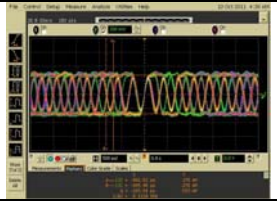
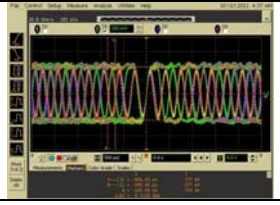
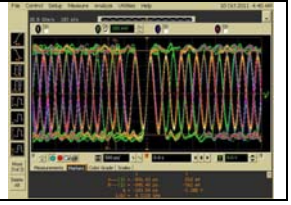


Figure4 PI2EQX6811 test setup for different output swing setting

Table2 Output Swing at TP4 vs. OS setting at 3Gb/s and 6Gb/s for PI2EQX6811

	OS[1..0]=00	OS[1..0]=01	OS[1..0]=10	OS[1..0]=11
Output Swing at TP4 vs. OS setting at 3Gb/s				
Output Swing at TP4 vs. OS setting at 6Gb/s				

Pre-emphasis Setting

Figure5 is PI2EQX6811 test setup for different Pre-emphasis setting, R is PI2EQX6811.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, EQ setting is 0dB

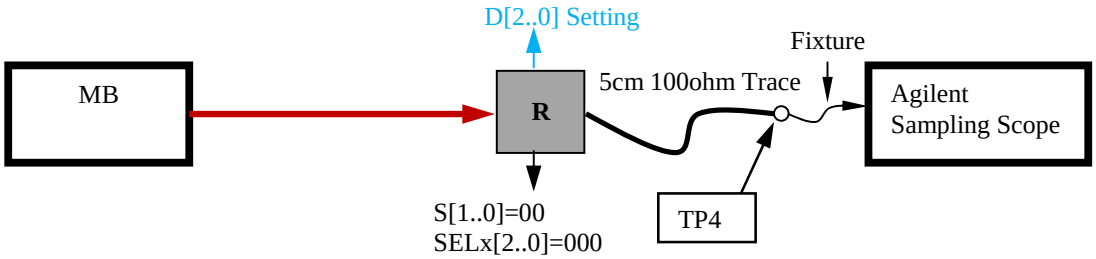
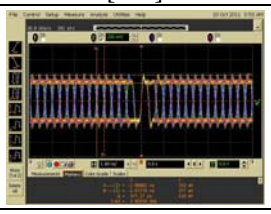
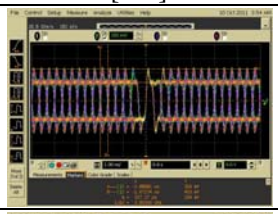
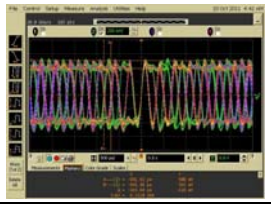
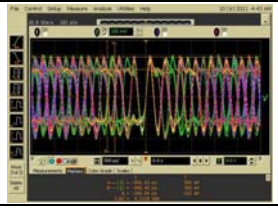


Figure5 PI2EQX6811 test setup for different Pre-emphasis setting

Table3 Pre-emphasis at TP4 vs. EM[1..0] setting at 3Gb/s and 6Gb/s for PI2EQX6811

	EM[1..0]=01	EM[1..0]=10	EM[1..0]=11
Output Pre-emphasis at TP4 vs. Pre-em setting at 3Gb/s			
Output Pre-emphasis at TP4 vs. Pre-em setting at 6Gb/s			

I2C Configuration Sequence

Figure6 is WRITE sequence.

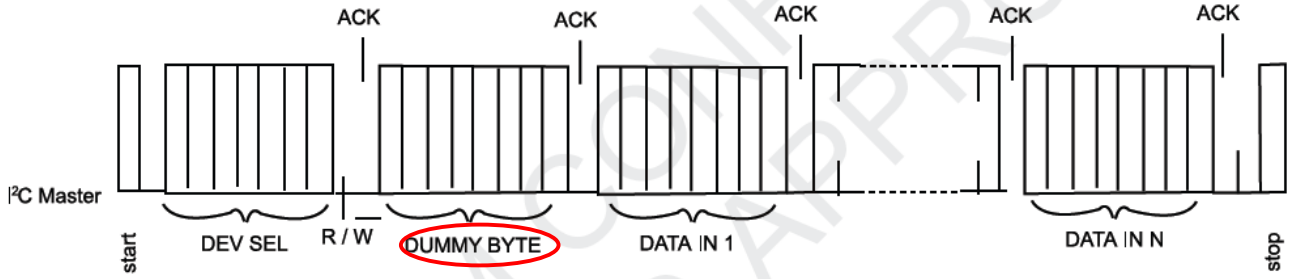


Figure6 I2C WRITE Sequence Diagram

Note: there is one DUMMY byte to be added into sequence.

Figure 7 is one sample for write sequence at Address=**C0** (A1, A0 are pulled down) and Data byte[0..14]=00,14,14,64,B0,C0,90,00,00,00,00,00,00,00,00,00.

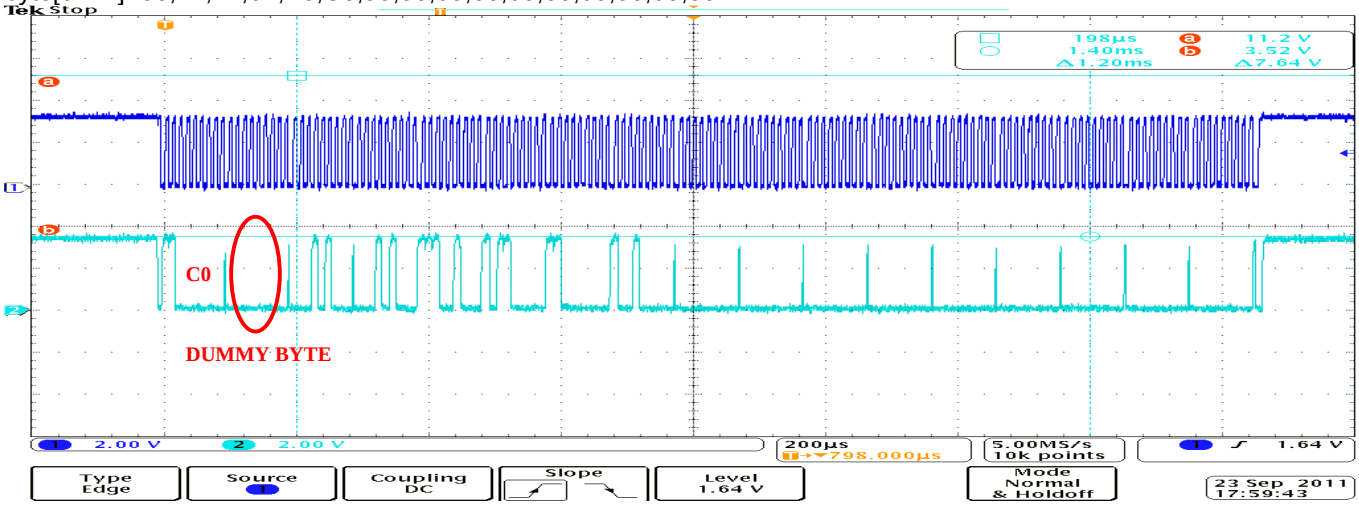


Figure7 I2C WRITE Sequence Sample

Figure8 is READ sequence.

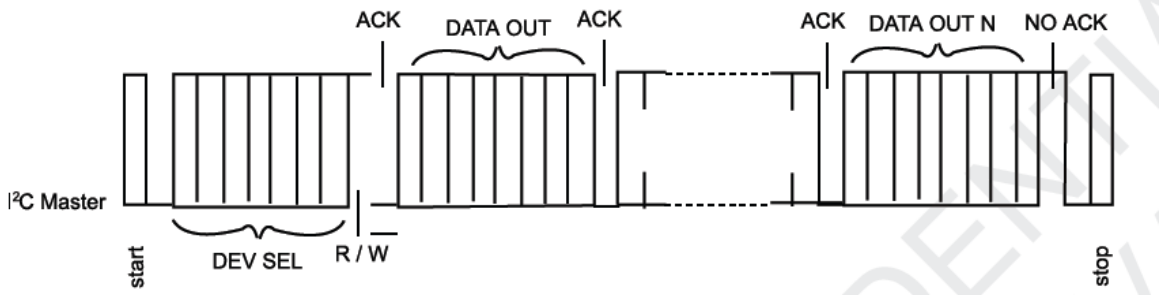


Figure8 I2C READ Sequence Diagram

Note: there is NO DUMMY byte to be added into sequence.

Figure9 is one sample for read sequence sample at Address=**C1** (A1, A0 are pulled down) and Data byte[0..14]= 14,14,64,B0,C0,90,00,00,00,00,00,00,00,00,00.

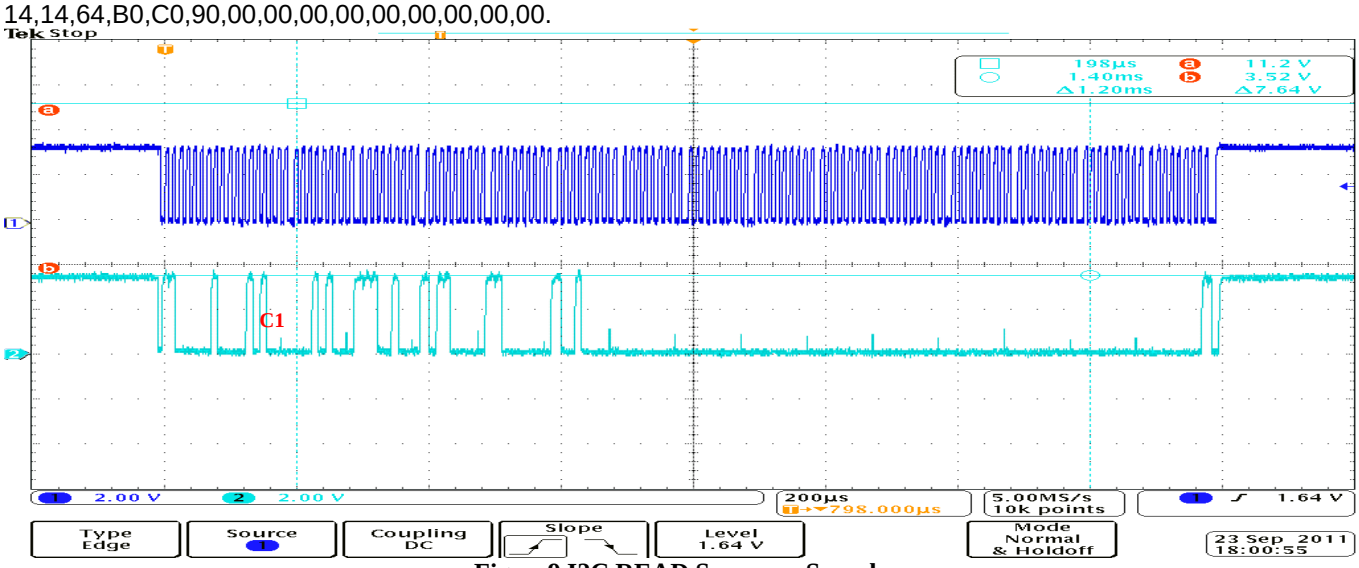
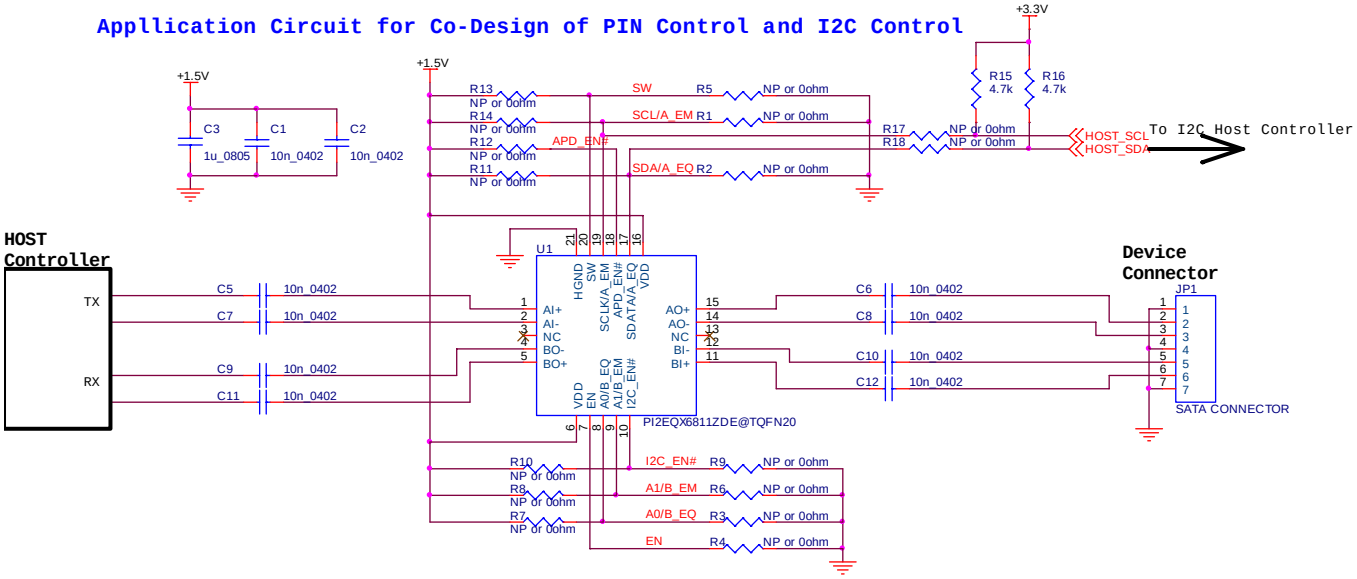


Figure9 I2C READ Sequence Sample

Typical Application Circuit

Figure10 shows typical application circuit of PI2EQX6811.



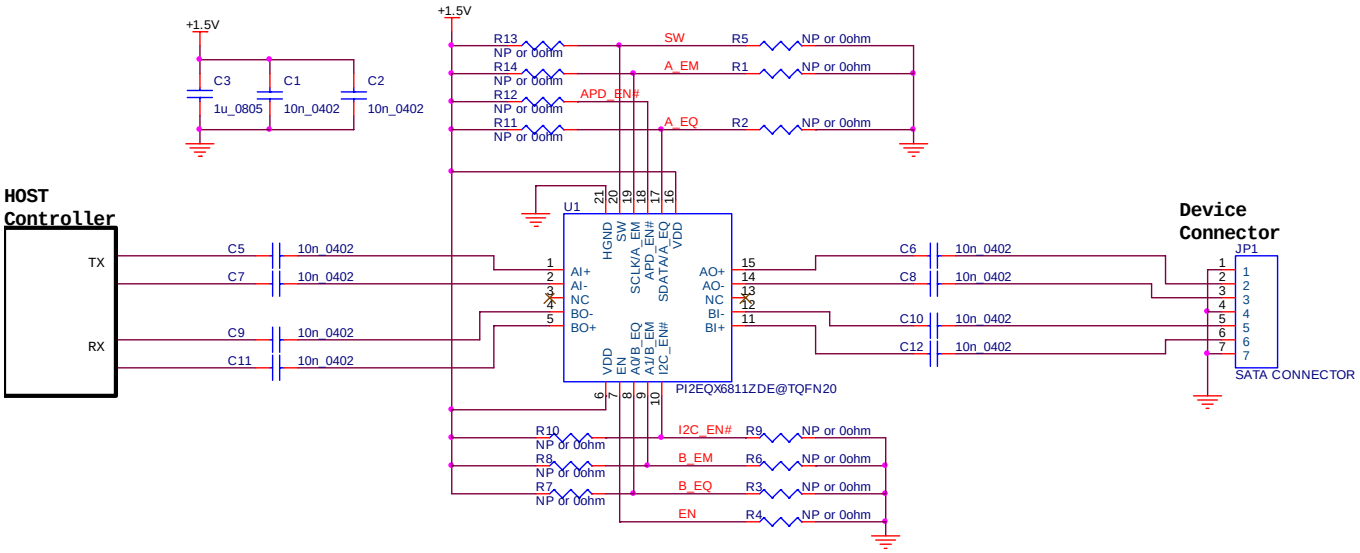
PIN CONFIGURATION for CONTROL

PIN NAME	PIN Control FUNCTION	I2C Control Function
P7:EN	With Internal 100k-ohm pull-up resistor High: Normal Operation Low: Power Down Mode R4=NP	Same as Pin control function R4=NP
P8:A0/B_EQ	Input Equalization for Channel B Tri-level control GND: 8dB R3=0ohm, R7=NP Open: 4dB R3=NP, R7=NP VDD: 16dB R3=NP, R7=0ohm	I2C Programmable address bit A0 R3 and R7 for A0 selection
P9:A1/B_EM	Pre-emphasis control for Channel B Tri-level control GND: 2dB R6=0ohm, R8=NP Open: 0dB R6=NP, R8=NP VDD: 3.5dB R6=NP, R8=0ohm	I2C Programmable address bit A1 R6 and R8 for A1 selection
P10:I2C_EN#	I2C Enable High: pin control R10=0ohm, R9=NP Low: I2C control R10=NP, R9=0ohm	Same as Pin control function
P17: SDATA/A_EQ	Input Equalization for Channel A R2 and R11 Tri-level control by R2 and R11 R18=NP Setting Value same as P8	I2C Data Line R2 and R11=NP R18=0ohm
P18:APD_EN#	Auto stumber mode Enable High: disable Low: enable	Don't Care
P19: SCLK/A_EM	Pre-emphasis control for Channel A R1 and R14 Tri-level control by R1 and R14 R17=NP Setting Value same as P9	I2C Clock Line R1 and R14 R17=0ohm
P20:SW	Output Swing control for Channel A&B Tri-level control GND: 667 mV(Vtx diff pp) at 3Gb/s R5=0ohm, R13=NP Open: 533 R5=NP, R13=NP VDD: 900 R5=NP, R13=0ohm	Don't Care

Figure10 Typical Application Circuit of PI2EQX6811

Figure11 shows typical application circuit of PI2EQX6811 for PIN Control function.

Application Circuit for PIN Control

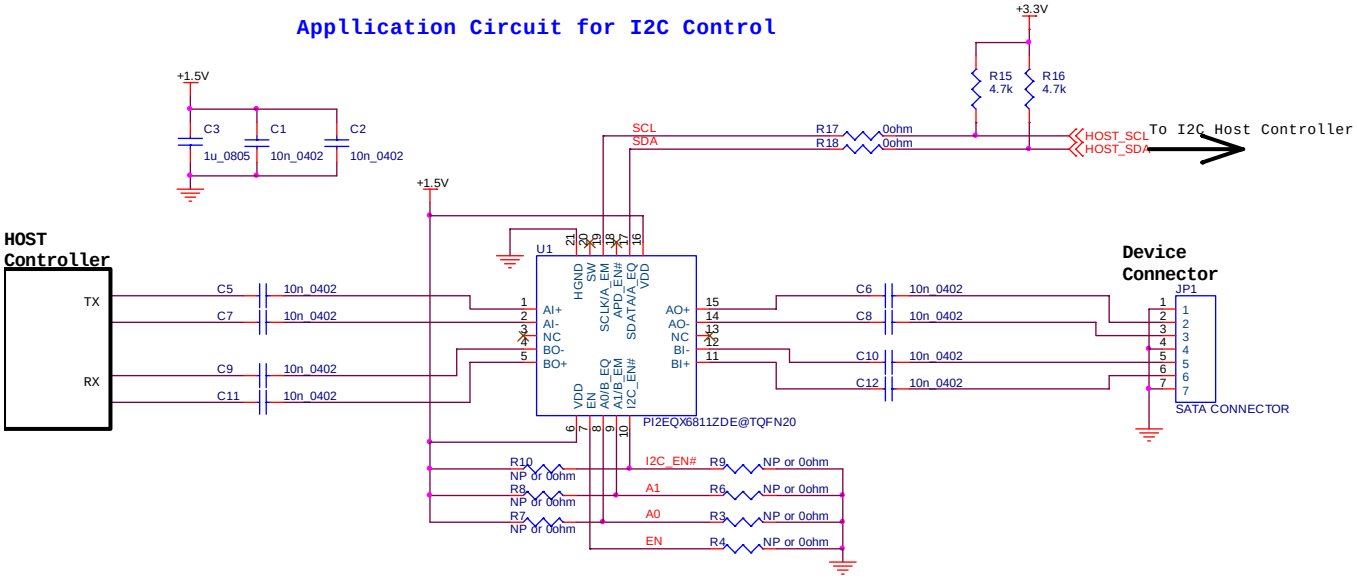


PIN CONFIGURATION for CONTROL

PIN NAME	PIN Control FUNCTION
P7:EN	With Internal 100k-ohm pull-up resistor High: Normal Operation Low: Power Down Mode R4=NP
P8:A0/B_EQ	Input Equalization for Channel B Tri-level control GND: 8dB R3=0ohm, R7=NP Open: 4dB R3=NP, R7=NP VDD: 16dB R3=NP, R7=0ohm
P9:A1/B_EM	Pre-emphasis control for Channel B Tri-level control GND: 2dB R6=0ohm, R8=NP Open: 0dB R6=NP, R8=NP VDD: 3.5dB R6=NP, R8=0ohm
P10:I2C_EN#	I2C Enable High: pin control R10=0ohm, R9=NP Low: I2C control
P17: SDATA/A_EQ	Input Equalization for Channel A R2 and R11 Tri-level control by R2 and R11 Setting Value same as P8
P18:APD_EN#	Auto stumber mode Enable High: disable Low: enable
P19: SCLK/A_EM	Pre-emphasis control for Channel A R1 and R14 Tri-level control by R1 and R14 Setting Value same as P9
P20:SW	Output Swing control for Channel A&B Tri-level control GND: 667 mV(Vtx diff pp) at 3Gb/s R5=0ohm, R13=NP Open: 533 R5=NP, R13=NP VDD: 900 R5=NP, R13=0ohm

Figure11 Typical Application Circuit of PI2EQX6811 for PIN control

Figure12 shows typical application circuit of PI2EQX6811 for I2C Control function.



PIN CONFIGURATION for CONTROL

PIN NAME	I2C Control Function
P7:EN	Same as Pin control function R4=NP
P8:A0/B_EQ	I2C Programmable address bit A0 R3 and R7 for A0 selection
P9:A1/B_EM	I2C Programmable address bit A1 R6 and R8 for A1 selection
P10:I2C_EN#	Same as Pin control function R10=NP, R9=0ohm
P17: SDATA/A_EQ	I2C Data Line R18=0ohm
P18:APD_EN#	**Don't Care**
P19: SCLK/A_EM	I2C Clock Line R17=0ohm
P20:SW	**Don't Care**

Figure12 Typical Application Circuit of PI2EQX6811 for I2C Control

PCB Layout Sample

Figure12 shows typical layout routing of PI2EQX6811.

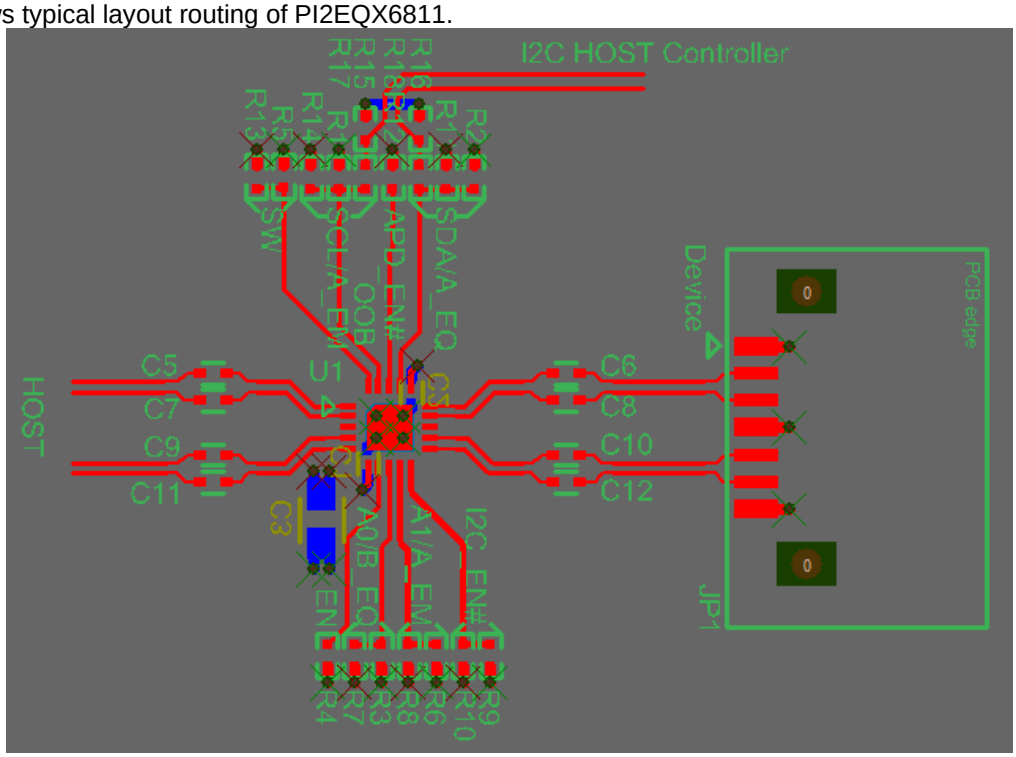


Figure12 Typical Layout Routing of PI2EQX6804-A

History

Version 1.0	Original Version	Nov. 2, 2011