White Paper

November 2021

Diodes' Holistic Solution to Ultra-High-Power-Density Charger Design

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The battery capacity of mobile devices continues increasing to meet operation time requirements for killer applications such as 5G mobile phones and gaming notebook PCs. At the same time, consumers want the instant gratification that comes with longer battery life yet shorter charging times and smaller charger sizes.

This demand is spurring the development of ultra-high-power-density (UHPD) chargers that are able to deliver 65W to 140W output power.

To meet the technical and aesthetic requirements of UHPDs, charger manufacturers need to address how to achieve charger size miniaturization while considering the system bill-of-material (BOM), efficiency, thermal management, EMI, and manufacturability for a mass consumer market.

These challenges are further complicated by a constantly moving goal, due to innovations in power components (e.g., GaN switches) and the dynamic market conditions. Furthermore, any local optimization of system performance in one specific area might not be optimal for the overall UHPD market, when measured against technical or business benchmarks.

Modern USB Type-C® UHPD chargers typically consist of two main stages: the Power Stage, which converts an AC power source to the DC output, and a protocol Decoder Stage, which provides the interface and handshaking for the device being charged. The correct voltage and current is negotiated between the two devices and delivered through the connector (e.g., CC1, CC2 for USB Type-C). It is the interaction between the Decoder and Power Stages that ensures the correct voltage and current appears on the output pins of the connector (Vbus).

Choice of Power Topology

Predominantly, a flyback power supply topology is used for chargers in the range of 65W to 140W. Flyback designs have known weaknesses, which present two areas for potential efficiency improvements. These are:

1) Leakage Inductance Energy losses due to the Passive Clamp RCD snubber circuitry *(Figure 1)*, which is used to suppress voltage spikes when the low-side main switch is turned off.

2) Switching losses due to overlap between the drain voltage and drain current. This occurs when the low-side main power switch is turned on and off *(Figure 2)*.

By addressing these inefficiencies in traditional flyback charger implementation, charger manufacturers can achieve considerable improvements in their UHPD chargers.

To support this, Diodes Incorporated favors an active clamp flyback (ACF) approach (*Figure 3*), which has two key features:

1) It provides Leakage Inductance Energy Recycling through the ACF circuitry.

2) It minimizes drain voltage when the switches turn on, ideally by using zero voltage switching (ZVS).

Figure 1. **Passive Clamp Snubber Burn Off Leakage Energy**

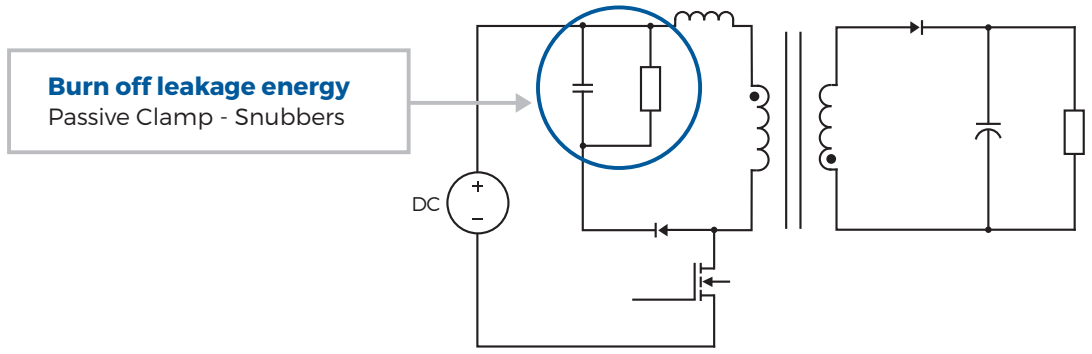


Figure 2. **Switching Loss due to Hard-Switching Main Switch**

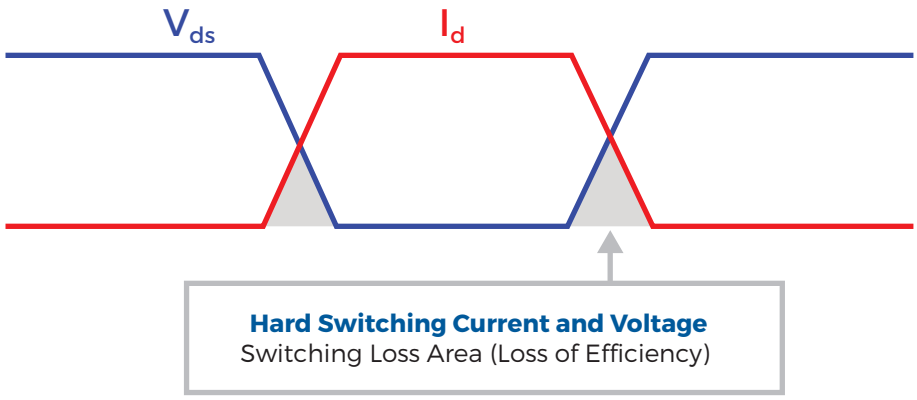


Figure 3. **Diodes' ACF Control Mechanism**

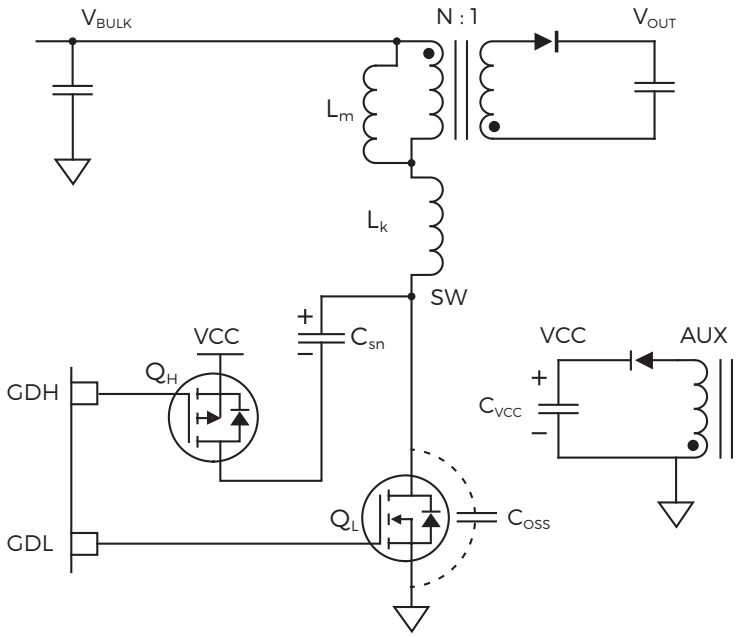
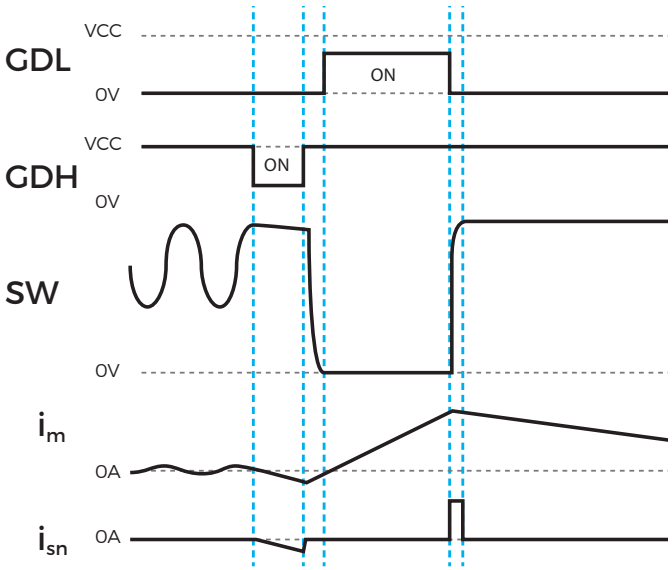


Figure 4. **Diodes' ACF Control Mechanism Waveform**



The principle of operation of the ACF circuit is as follows:

1) When the main MOS switch, Q_L, turns off, the current in the leakage continues to flow and charge the ACF capacitor through the body diode of the high-side MOS switch, Q_H. The energy stored in the capacitor will be used later for ZVS operation.

2) The ACF controller senses the drain voltage by monitoring the demag pin and looking for the drain voltage peak while it is in resonant ringing. This operation is very similar in principle to valley switching for quasi-resonant (QR) topologies.

3) The high-side MOS switch, Q_H, turns on at the peak voltage of the SW node (drain voltage of the main switch). At this point, energy stored in the ACF capacitor is released and current flows into the primary winding of the transformer.

   The on-time of the high-side switch is self-adjusted to suit different line voltage and output voltage operating conditions.

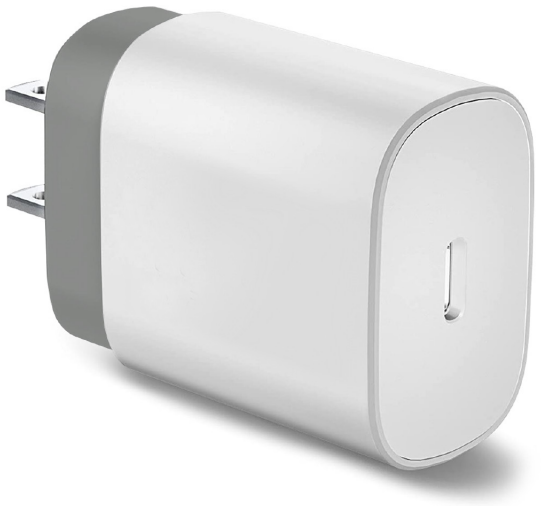
4) The high-side MOS switch, Q_H, turns off when the optimal on-time is reached. The current flowing into the primary winding continues to pull the SW node low until the SW node is close to 0V for ZVS operation. The dead time is optimized to support ZVS operation.

5) The main MOS switch, Q_L, turns on when the voltage on the SW node is close to 0V, to minimize switching losses. The on-time of the QL is controlled by the loop to reflect correct energy delivery.

6) The operation is repeated for the next ACF cycle.

The ACF circuit can be adapted to support either MOS or GaN switches in both high-side and low-side positions.

GaN switches are gaining popularity due to their higher operating frequency, lower capacitance, and lower $R_{DS(ON)}$.



While their driving mechanism is very different from MOS switches, ACF PWM controllers with high-side and low-side drivers that can support GaN switches are commercially available.

Such controllers operate at high frequencies of 400 kHz or more, and are aimed at UHPD chargers.

While these solutions might attract some early adoption, they do not address the other critical considerations for consumer chargers, as outlined above.

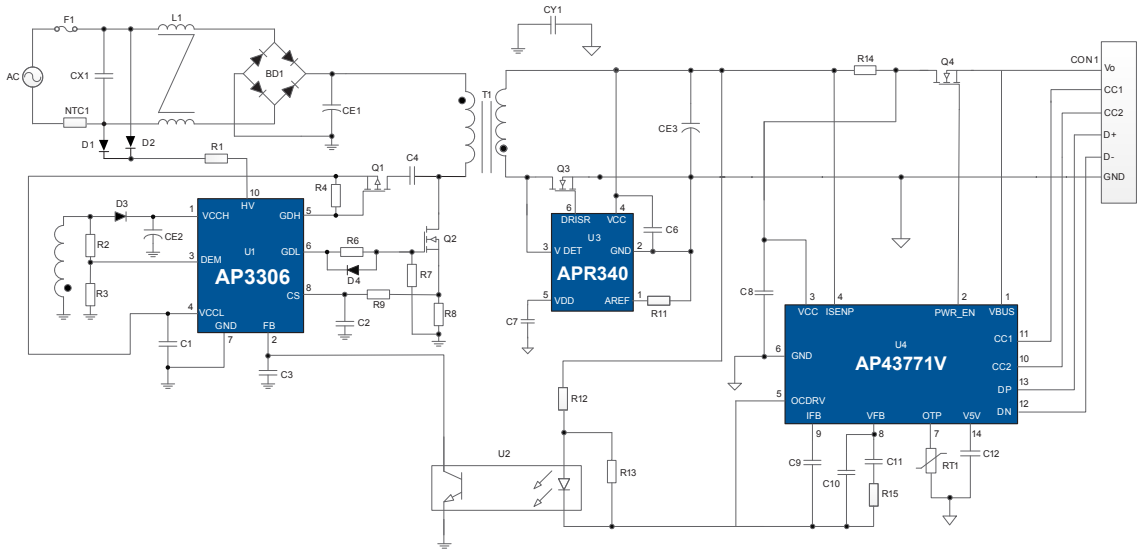
These include cost-effectiveness, meeting EMI challenges, and designing for high volume manufacturability to target the 65W UHPD charger opportunity.

In order to help manufacturers overcome these challenges, Diodes has developed a reference design for 65W ACF chargers.

It features a power stage based on the AP3306 ACF PWM controller, a high-side pMOS switch, and a low-side nMOS switch.

The circuit operates in the range of 100 kHz to 160 kHz and provides an optimal system BOM for mass consumer charger applications *(Figure 5)*.

Figure 5. **Schematics of 65W Active Clamp Flyback Charger**



The synchronous rectification (SR) in the secondary side of the flyback chargers is also crucial to the overall system efficiency of the power stage design.

With this consideration, Diodes has developed a family of SR controllers: the APR34X family. The APR340 supports QR, CCM, and ACF operating modes.

Implementing UHPD Protocol Decoding

The USB PD3.0 PPS specification is commonly used in UHPDs. Its use presents practical issues related to the power stage of a quick charger, which includes various technical and commercial requirements:

1) Wide output voltage range: 3.3V to 21V, up to 3.25A (65W)
2) Integration of high-voltage start-up circuitry at extremely low standby power (<30mW)
3) Integration of X-capacitor discharging circuitry
4) Dynamic behavior to meet switching time requirements for voltage switching
5) Customization per application power profile for protocol decoders
6) USB PD3.0 PPS certification
7) The lowest system BOM

Implementing UHPD Protocol Decoding (cont)

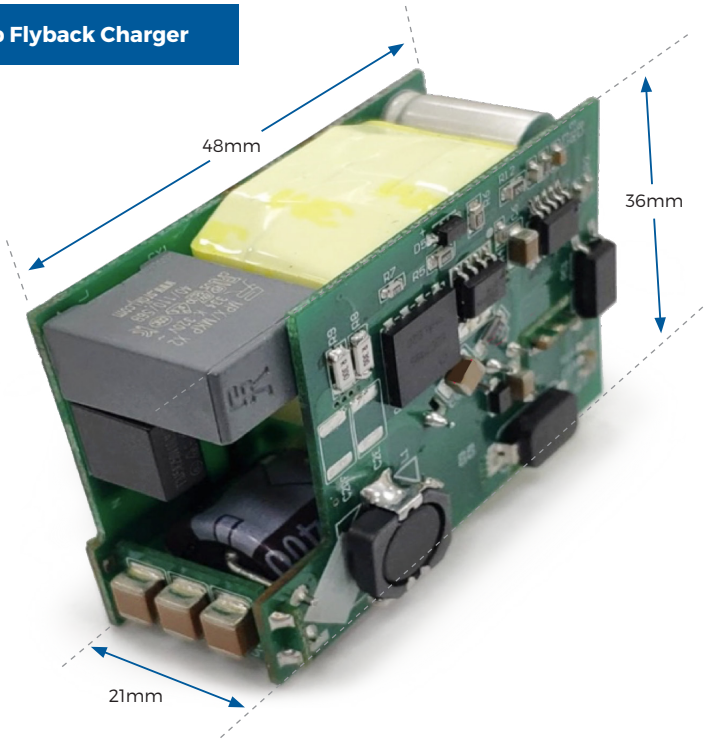
To meet these requirements, Diodes has developed the AP43771V (QFN-14, QFN-24 with I2C interface) family for single-port or multiple-port quick-charging systems.

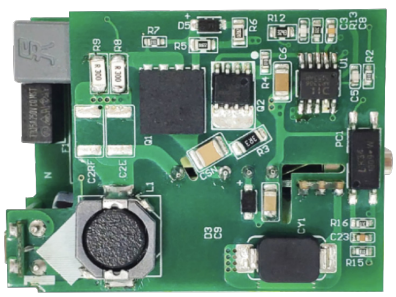
The controller integrates an embedded MCU with one-time-programmable (OTP) memory, which can store the protocol decoder firmware. The AP43771V also provides a virtual multi-time programmable (MTP) area for customization, supporting different quick-charger power profiles. It is supported by development tools for programming the AP43771 MTP firmware up to four times.

The 65W ACF charger reference design *(Figure 6)* based on the AP43771V supports the full-power range for PD3.0 PPS applications. Table 1 and Table 2 summarize the key performance figures of the 65W ACF charger reference design.

Figure 6. **65W Active Clamp Flyback Charger**

System Configuration
AP3306 (ACF Controller)
+ **DMP65H09D** (ACF High-Side Switch)
+ **APR340** (SR Controller)
+ **AP43771V** (DFN-14, PD3.0 PPS Decoder)





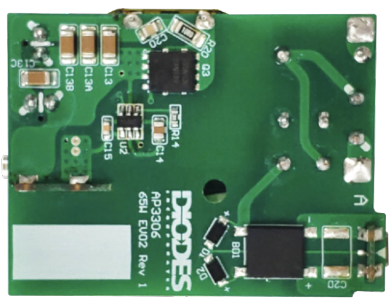


Table 1. 65W Active Clamp Flyback Charger Summary

Parameter	Value
Input Voltage	$90V_{AC}$ to $264V_{AC}$
Input Standby Power	< 30mW
Main Output	**PDO:** 5V/3A, 9V/3A, 15V/3A, 20V/3.25A,
(Vo / Io)	**APDO:** 3.3V to 21V/3A
Voltage Step	PPS 20mV step voltage, 3.3V-21V
Efficiency	Comply with CoC version 5 tier-2
Total Output Power	65W (at PDO 20V/3.25A)
Protections	OCP, OVP, UVP, OLP, OTP, SCP
Dimensions	**PCB:** 36 * 48 * 21 mm^3, 1.417" * 1.89" * 0.827" $inch^3$ **Case:** 40 * 52 * 25 mm^3, 52CC, 3.17 CI
Power Density Index	1.25 W/CC; 20.48 W/CI

Table 2. 65W Active Clamp Flyback Charger Key Performance Parameters

Parameter	Value	Test Summary
Input Voltage / Frequency	$90V_{AC}$ to $264V_{AC}$ / 50Hz or 60Hz	Test Condition
Input Current	$<2A_{RMS}$	
Standby Power	< 30mW, load disconnected	**PASS** 16.85mW@$230V_{AC}$/50Hz
5V/3A Average Efficiency	CoC Version 5, Tier-2 Efficiency >81.84%	**PASS** 91.14%@$115V_{AC}$/60Hz 89.81%@$230V_{AC}$/50Hz
5V/0.3A Efficiency (10% Load)	CoC Version 5, Tier2 Efficiency >72.48%	**PASS** 87.97%@$115V_{AC}$/60Hz 87.23%@$230V_{AC}$/50Hz
9V/3A Average Efficiency	CoC Version 5, Tier2 Efficiency >87.30%	**PASS** 92.74%@$115V_{AC}$/60Hz 92.19%@$230V_{AC}$/50Hz
9V/0.3A Efficiency (10% Load)	CoC Version 5, Tier2 Efficiency >77.30%	**PASS** 89.42%@$115V_{AC}$/60Hz 88.75%@$230V_{AC}$/50Hz
15V/3A Average Efficiency	CoC Version 5, Tier2 Efficiency >88.85%	**PASS** 93.14%@$115V_{AC}$/60Hz 93.02%@$230V_{AC}$/50Hz
15V/0.3A Efficiency (10% Load)	CoC Version 5, Tier2 Efficiency >78.85%	**PASS** 90.71%@$115V_{AC}$/60Hz 87.59%@$230V_{AC}$/50Hz
20V/3.25A Average Efficiency	CoC Version 5, Tier2 Efficiency >89%	**PASS** 93.15%@$115V_{AC}$/60Hz 93.18%@$230V_{AC}$/50Hz
20V/0.325A Efficiency (10% Load)	CoC Version 5, Tier2 Efficiency >79%	**PASS** 90.07%@$115V_{AC}$/60Hz 88.54%@$230V_{AC}$/50Hz
Output Voltage Regulation Tolerance	+/- 5%	**PASS**
16V PPS	3.3V – 16V +/- 5%, 0~2.8A +/-150mA	**PASS**
21V PPS	3.3V – 21V +/- 5%, 0~2.1A +/-150mA	**PASS**
Conducted EMI	>6dB Margin; according to EN55032 Class B	

Conclusions

The pace of innovation and system optimization for UHPD chargers has accelerated, thanks in part to the introduction of new, high-performance power components.

Based on an optimized ACF implementation with high-side and low-side MOS switches, Diodes has developed a complete UHPD reference design that covers the range of 65W to 140W output power, meeting the mass market requirements.

The 65W ACF (52CC volume) UHPD charger reference design shown here illustrates the value proposition. Diodes can supply other ACF reference designs to support specific customer requirements.

The advantages of GaN switches over MOS switches in power supply applications have attracted significant investment and, as a result, eroded the price premium over traditional MOS switches.

This makes GaN even more attractive for UHPD charger applications.

Meanwhile, demand for multiple-port USB Type-C charging applications is also driving new system optimizations in the protocol decoder stage of UHPD chargers.

Power IC manufacturers must accelerate their pace of innovation, with a holistic approach to ensure that optimal UHPD chargers continue to meet mass consumer market demand.

Related information

- **AP3306** - https://www.diodes.com/part/AP3306
- **APR340** - https://www.diodes.com/part/APR340
- **AP43771V** - https://www.diodes.com/part/AP43771V
- **65W Active Clamp Flyback Reference Design EVB1/2**
  - www.diodes.com/assets/Evaluation-Boards/65W-ACF-PD3.0-PPS-Adapter-EVB1-User-Guide-Released-1.0.pdf
  - www.diodes.com/assets/Evaluation-Boards/65W-ACF-PD3.0-PPS-Adapter-EVB2-User-Guide-Released-1.0.pdf