Table of Contents

Chapter 1. CLM EVB Summary

1.1 Introduction of CLM EVB

To expedite a USB-C port connected Device (TCD) to display its video signal to a DisplayPort™ (DP) monitor through USB-C interface, a USB-C-Link-to-DP-Monitor Evaluation Board (CLM EVB) is designed, where its functions include the USB-C Power Delivery (PD) charging, DP Alternate (Alt) mode, and USB 3.1 data streaming. The key functions of the CLM EVB are shown in Figure 4, where the CLM EVB can support PD 3.1 compliant TCDs such as notebook PC, Smartphone, Desktop PC, and other mobile or non-mobile devices.

1.2 Key Features

The CLM EVB demonstrates 2 key functions: USB-C PD charging, and DP Alt mode support of video stream and USB 3.1 data.

To implement the PD 3.1 protocol and charging, a USB-IF compliant PD controller AP43781 is used. To support the DP Alt mode and USB data, the high speed switch PI3USB31531 and signal re-driver PI3DPX1207C are included. To deliver up to 100W of PD output power at USB-C port and provide 5V at Type-A port, the power stage uses a DC-DC buck-boost controller and a DC-DC buck converter AP63205, respectively.

1.2.1 AP43781 - USB PD Controller for USB-C Port in DP Monitor

- USB-C PD 3.1 SPR Compliance Protocol Controller
- Embedded MCU with hardwired PD protocol supports CC1/2 detection, traffic identification and routing requirements for PD compliance charging and data flow control
- Support DFP charging up to 100W (20V @ 5A)
- Support UPF DisplayPort over USB-C Alternate (DP Alt) mode and USB 3.1 Gen 1 / Gen 2
- Configure I2C Slave devices to support PD charging, video and data routing through I2C interface
- OVP, OCP, UVP Protection

1.2.2 PI3USB31531 - Crossbar Switch for USB-C 3.1 Gen1 /Gen 2 / DP1.4

- Six Differential Channels to 2/4 Differential Channel Switch
- Support Pin Assignment C, D, E for Sink
- USB 3.1 Gen 1 - 10Gbps/s (-3db) for Super Speed and (-3.7db) Switching to USB-C Connector
- Multiplexes one of the following to USB-C
- One Lane of USB 3.1 Gen 1/Gen 2 Signal and Channels of DP1.2 / DP1.4 Channels of Signal

1.2.3 PI3DPX1207C - DP-Alt DP1.4 / USB 3.1 10Gbps Re-Driver

- DP-Alt 4-channel Re-driver and De-Mux (DP 2-ch and USB 2-ch)
- DP1.4 (8.1Gpbs) and USB 3.1 Gen 2 (10 Gbps) standard compliance
- USB-C DP/USB mode selection: DP only, USB only, DP/USB split modes
- USB-C Plug and Aux Flipping control through I2C slave pins

1.3 Applications

- DRP USB-C Port USB-C Interface Model for PC Monitors, TVs and USB Hubs

1.4 Main Power Specifications

Parameter	Value
Panel Interface	USB-C, DP
Applicable USB-C Devices (TCDs)	USB-C PD Equipped Notebook, Desktops, Smartphones, PADs
Input Operating Voltage	12~20 Vdc
Output Charging Power	USB-C PD 100W Maximum Output Power (20V@5A);
Charging Efficiency	94.64% (5V @ 3A) 94.93% (20V @ 5A)
Video/Data Support	USB-C Alt Mode – 2-lane/4-lane DP USB 3.1 Gen 1 / Gen 2
Standby Power	< 40mWatt
Dimension	75mm * 75mm * 14mm

1.5 CLM EVB Picture

Figure 1. Top View

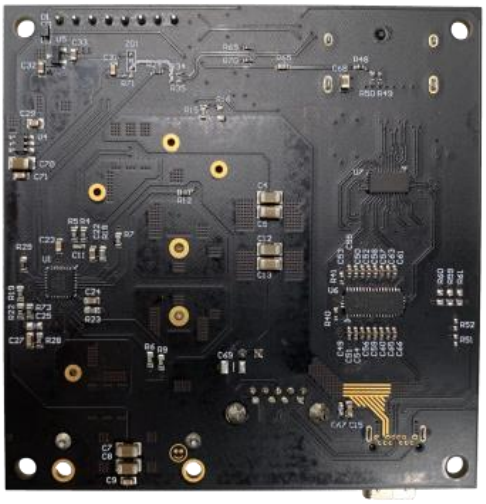


Figure 2. Bottom View

Chapter 2. Function Description, Schematic and BOM

2.1 Application Scenario

With emerging USB-C connectors and PD capability available, new generations of USB-C PD PC monitors can be used as both a power source and a data hub for personal and professional PC work environment. While a USB-C PD monitor is the only device plugged in wall outlet for AC power inputs, it plays as data UFP (Upstream Facing Port) to the connected to TCDs (e.g. Notebook, PAD, Phone) as well as DC power DFP (Downstream Facing Port) for the required power in the monitor. Once the DFP DC power is delivered, the monitor and the TCD swaps data role. Playing as the DFP role, the TCD requests the UFP monitor to support the DP Alt mode so that the DP video signal can go to the DP monitor properly. Figure 3 illustrates a usage set up for PC Notebook and PC monitors in typical PC working scenarios.

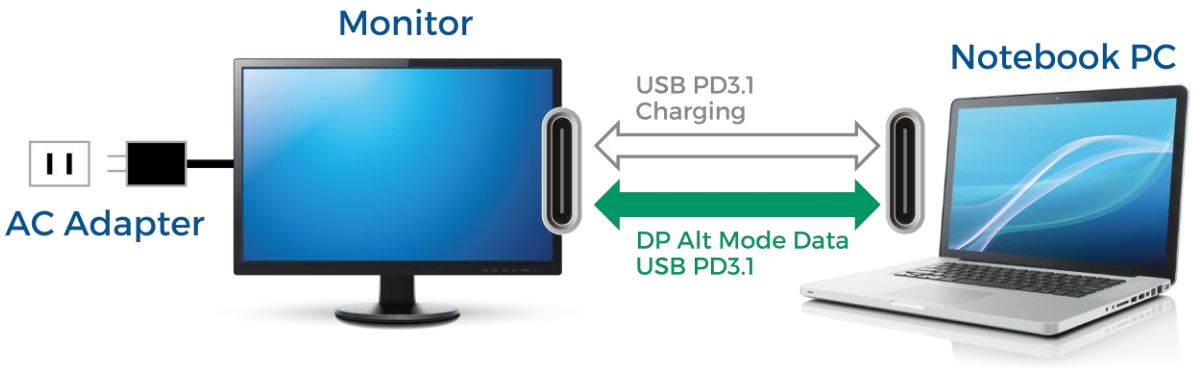


Figure 3. The Application Scenario of a USB-C PD Charging and Video Data Streaming

The USB-C PD monitor system block can be divided into four main functions:

1. Power Unit (conversion of AC Power into Desired DC Power)
2. Major Image Processing and Display SoC (Image formatting and scaling)
3. USB hub controller (support various USB devices)
4. USB-C PD Interface (dealing with PD charging and data/video signaling and routing)

The CLM EVB, Figure 4, is designed to implement the USB-C PD Interface for USB-C PD monitor.

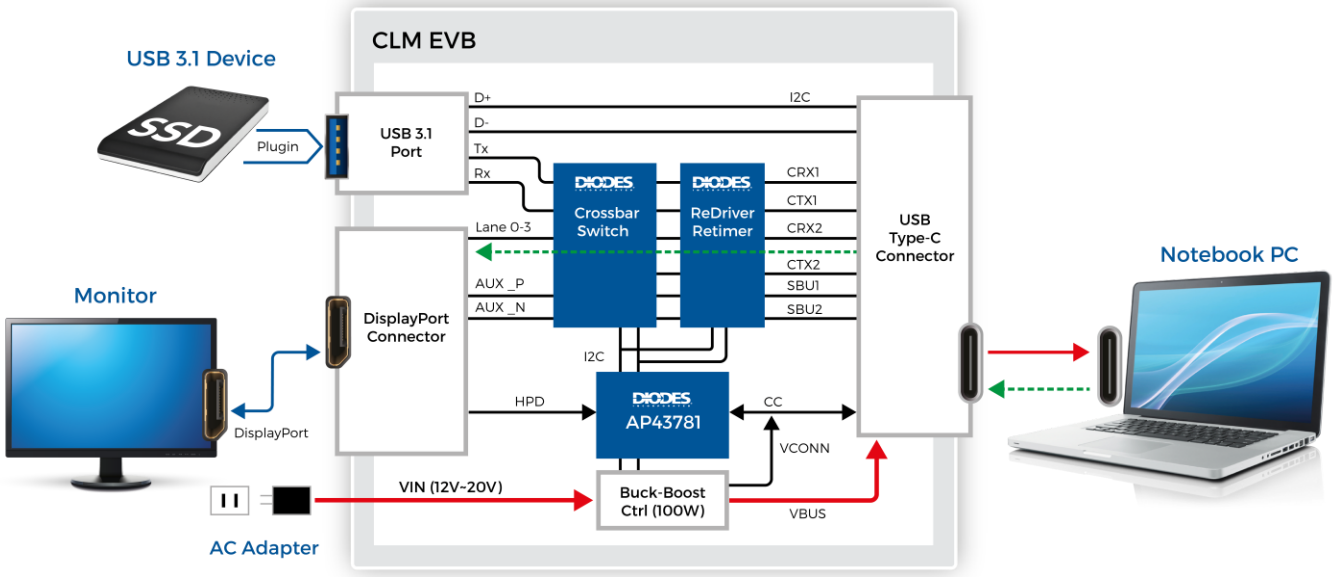


Figure 4. An AP43781-based EVB for USB-C PD DFP Charging and UFP Video Data Streaming

2.2 Functional Description

The CLM EVB is designed to input a DC power of range 12V~20V, which is supplied by an AC-to-DC power conversion module board inside the Monitor with AC Power input from the AC wall outlet, as illustrated in Figure 4. This application operates in the following modes:

- 100W DFP charging port with UFP supported for DP Alt mode:
  When the USB-C port is connected to a Notebook or a Mobile Phone by an USB-C cable, CLM EVB sources up to 100W power for charging the Notebook or the Phone. Then CLM EVB swaps to be an UFP to support the monitor with DP Alt mode output to the DisplayPort connector, and the USB device (SSD) to the USB connector.

- Self-powered UFP supported for DP Alt mode:
  When the USB-C port is connected to a Desktop PC by an USB-C cable, the CLM EVB acts as a self-powered UFP to support the monitor with DP Alt mode output to the DisplayPort connector, and the USB device (SSD) to the USB connector.

To support desired PD 3.1 charging and data/video signaling and routing for DP Alt mode, the CLM EVB adopt the following key components:

1) DisplayPort over USB-C Capable PD Controller (**AP43781** - USB PD controller supporting DP Alt mode.)
2) I2C Buck-Boost Controller (capable to support up to 100W PD charging, 20V@5A)
3) I2C USB-C Re-driver (**PI3DPX1207C** - DP-Alt DP1.4/USB3.1 10Gbps linear re-driver with non-blocking, latency-free and built-in aux switch)
4) I2C 6:4 Cross-Bar Switch (**PI3USB31531** - 3.3V, USB-C USB3.1 Gen 2/DP1.4 6:4 Crossbar Switch)
5) I2C IO Expander chip (**PI4IOE5V9554** - 8-bit I2 C-Bus and SMBus I/O Port with Interrupt)

When the USB-C attachment is completed between an active CLM EVB and the NB host, the power profile negotiation begins with a series of Channel Configuration (CC) commands and response exchanges. Upon successful negotiation, the power profile selection is concluded. The AP43781 enables the attached I2C buck-boost controller to output the matched PDO (Power Data Object) power to charge the NB host.

Once the charging is conducted, the AP43781 sends the data role swap request to the NB host. If the request is accepted, the NB host plays as DFP, and starts to request the UFP AP43781 to support the DP Alt mode. Upon successful decoding the Vendor-Defined Message (VDM) commands on the CC line driven by NB host, the AP43781 enters the DP Alt mode. The decoded information is then sent to the high speed switches and re-timer/re-driver signaling chips through the AP43781

I2C interface, so that the data stream can be delivered from the host side to the DP in the right routing path and in the correct signaling, as the green color line illustrated in Figure 4.

During the video and data inquiry process, the AP43781 identifies proper Pin Assignment (C, D, E, 2-lane/4-lane DisplayPort, 1-lane USB 3.1, 2-lane DP+1-Lane USB) to match various attached output devices (e.g. Monitor, or SSD), where it includes the routing information for the Cross-Bar Switches (e.g. PI3USB31531) and the signaling parameters for signal conditioning chip (e.g. PI3DPX1207C). In addition to its default value, the PI3DPX1207C can be set up via the crucial parameters (register values) according to PCB trace lengths (USB-C Connector to Re-Driver, Re-Driver to DP/USB port), types of incoming data/video and cable loss characteristic by the AP43781 through the I2C interface.

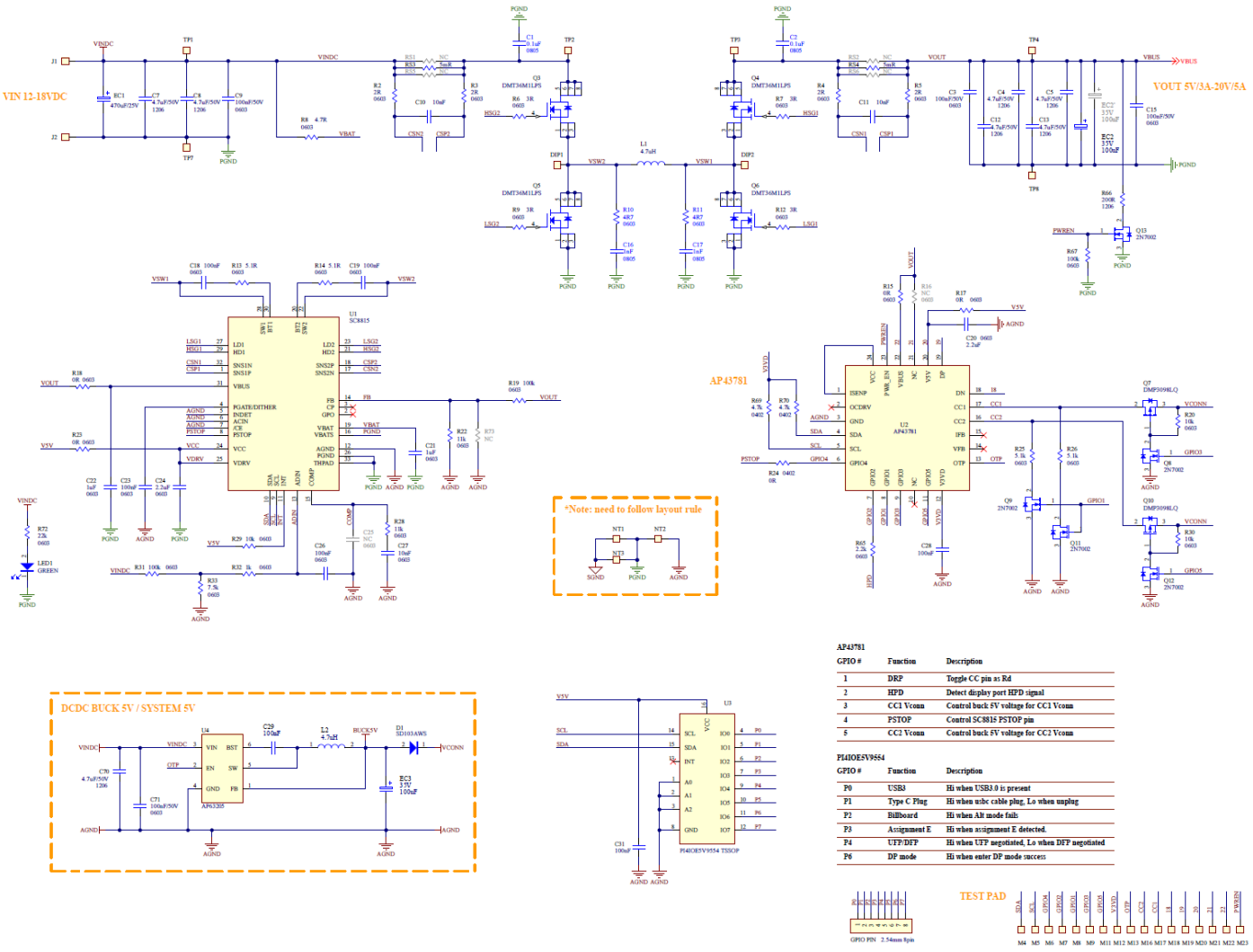
Considering the power requirements to support various USB-C active cables, the CLM EVB has an extra power circuitry based on synchronous buck regulation (AP63205) to support more than 2.0W power. If adequate power source in the main monitor board is available to support up to 2.0W power (5V), this extra active power circuitry can be saved.

To support development-debugging purposes, the CLM EVB adopts I2C IO Expander chip (PI4IOE5V9554) to monitor critical signals shown below:

GPIO #	Function	Description
P0	**USB 3**	High when USB 3.0 is present
P1	**USB-C Plug**	High when USB-C cable plug, Low when unplugged
P2	**Billboard**	High when Alt mode fails
P3	**Assignment E**	High when assignment E detected.
P4	**UFP/DFP**	High when UFP negotiated, Low when DFP negotiated
P5	**reserved**	For future use
P6	**DP mode**	High when enter DP mode success

Furthermore, the AP43781 also minimizes standby power consumption (<40mWatt, excluding I2C IO expander circuitry) of the overall CLM EVB to meet Energy Star® requirements on PC monitors.

2.3 CLM EVB Schematic



AP43781

GPIO #	Function	Description
1	DRP	Toggle CC pin as Rd
2	HPD	Detect display port HPD signal
3	CC1 Vconn	Control buck 5V voltage for CC1 Vconn
4	PSTOP	Control SC8815 PSTOP pin
5	CC2 Vconn	Control buck 5V voltage for CC2 Vconn

PI4IOE5V9554

GPIO #	Function	Description
P0	USB3	Hi when USB3.0 is present
P1	Type C Plug	Hi when usbc cable plug, Lo when unplug
P2	Billboard	Hi when Alt mode fails
P3	Assignment E	Hi when assignment E detected.
P4	UFP/DFP	Hi when UFP negotiated, Lo when DFP negotiated
P6	DP mode	Hi when enter DP mode success

Figure 5. Charging and Power Stage Circuitry with an I/O Expander (PI4IOE5V9554) to Show System Status

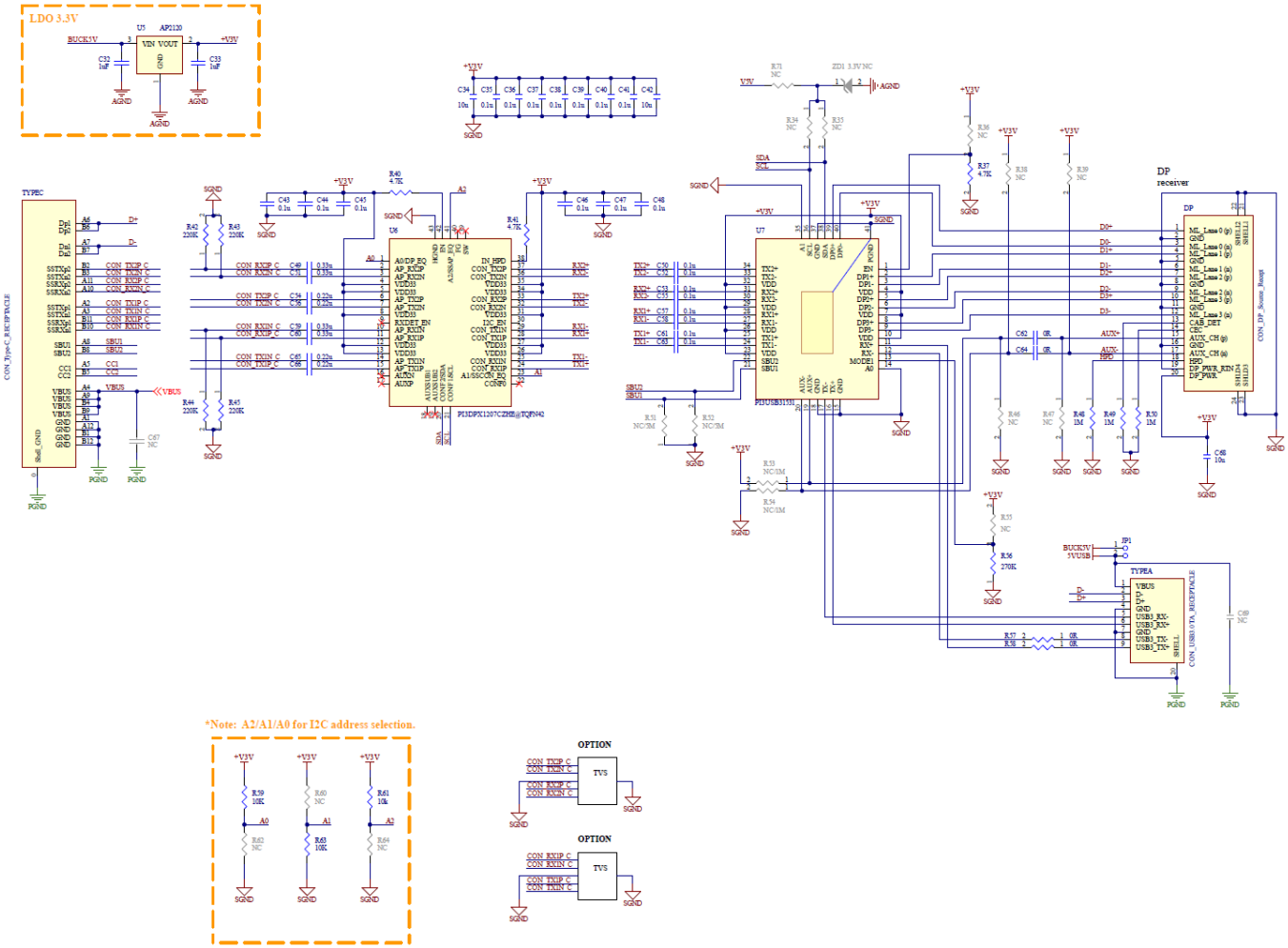


Figure 6. Video Signaling and Routing Related Circuitry with a Type-A to deliver USB data

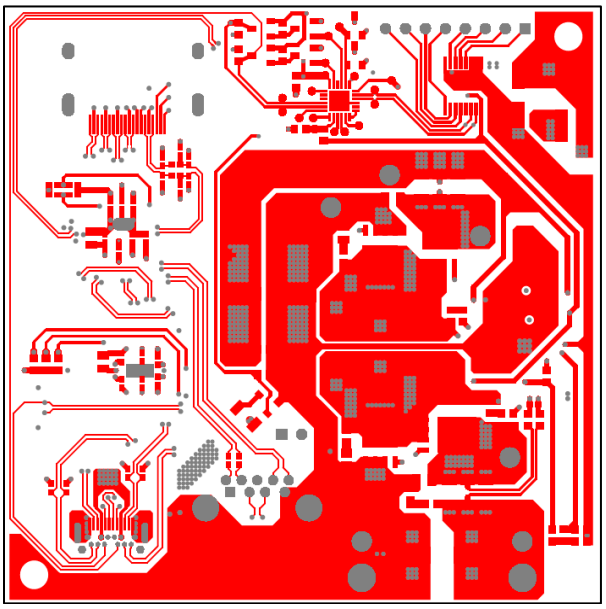
2.4 Bill of Material (BOM)

Item	Quantity	Designator	Description	Footprint	Manufactory
1	2	C1, C2	MLCC 0.1μF 50V 0805 X7R	C-0805	YAGEO
2	11	C3, C9, C15, C18, C19, C23, C26, C28, C29, C31, C71	MLCC 0.1μF 50V 0603 X7R	C-0603	YAGEO
3	7	C4, C5, C7, C8, C12, C13, C70	MLCC 4.7μF 50V 1206 X7R	C-1206	YAGEO
4	1	EC1	EC 470μF 25V 10X10.5	SMD 10x10.5	VT
5	2	EC2, EC3	EC 100μF 35V 6.3X7.7	SMD 6.3x7.7	ELNA
6	2	C10, C11	MLCC 10nF 50V 0402 X7R	C-0402	YAGEO
7	2	C16, C17	MLCC 1nF 50V 0805 X7R	C-0805	YAGEO
8	2	C20, C24	MLCC 2.2μF 25V 0603 X7R	C-0603	YAGEO
9	4	C21, C22, C32, C33	MLCC 1μF 25V 0603 X7R	C-0603	YAGEO
10	1	C27	MLCC 10nF 25V 0603 X7R	C-0603	YAGEO
11	3	C34, C42, C68	MLCC 10μF 16V 0805 X7R	C-0805	YAGEO
12	21	C35, C36, C37, C38, C39, C40, C41, C43, C44, C45, C46, C47, C48, C50, C52, C53, C55, C57, C58, C61, C63	MLCC 0.1μF 16V 0402 X7R	C-0402	YAGEO
13	4	C49, C51, C59, C60	MLCC 0.33μF 16V 0402 X7R	C-0402	YAGEO
14	4	C54, C56, C65, C66	MLCC 0.22μF 16V 0402 X7R	C-0402	YAGEO
15	2	C62, C64	RES 0R 0402 1%	C-0402	YAGEO
16	1	DP	MDP20-01-06	CON DP Receiver	MATRIX
17	1	GPIO PIN		2.54mm 8pin	
18	1	JP1		2.54mm 2pin	
19	1	L1	RCA-1265H-4R7M	4.7μH 12*12*6.5mm	RDM technology
20	1	L2	PI043-4R7M	4.7μH 4.5*4*3.2mm	JLS.IC
21	4	Q3, Q4, Q5, Q6	DMT36M1LPS-13	DFN 5x6	DIODES
22	2	Q7, Q10	DMP3098LQ	SOT23	DIODES
23	5	Q8, Q9, Q11, Q12, Q13	2N7002	SOT23	DIODES
24	4	R2, R3, R4, R5	RES 2R 0603 1%	R-0603	YAGEO
25	4	R6, R7, R9, R12	RES 3R 0603 1%	R-0603	YAGEO
26	3	R8, R10, R11	RES 4.7R 0603 1%	R-0603	YAGEO
27	2	R13, R14	RES 5.1R 0603 1%	R-0603	YAGEO
28	4	R15, R17, R18, R23	RES 0R 0603 1%	R-0603	YAGEO
29	3	R19, R31, R67	RES 100k 0603 1%	R-0603	YAGEO
30	3	R20, R29, R30	RES 10k 0603 1%	R-0603	YAGEO
31	2	R22, R28	RES 11k 0603 1%	R-0603	YAGEO
32	3	R24, R57, R58	RES 0R 0402 1%	R-0402	YAGEO
33	2	R25, R26	RES 5.1k 0603 1%	R-0603	YAGEO
34	1	R32	RES 1k 0603 1%	R-0603	YAGEO
35	1	R33	RES 7.5k 0603 1%	R-0603	YAGEO
36	5	R37, R40, R41, R69, R70	RES 4.7k 0402 1%	R-0402	YAGEO

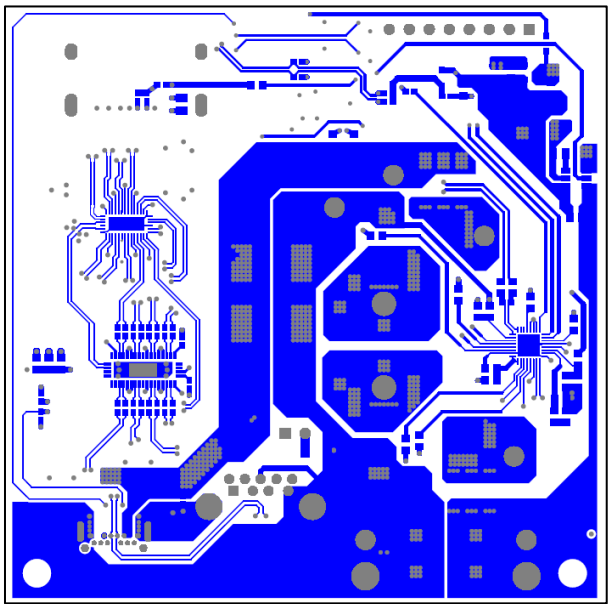
37	4	R42, R43, R44, R45	RES 220k 0402 1%	R-0402	YAGEO
38	3	R48, R49, R50	RES 1M 0402 1%	R-0402	YAGEO
39	1	R56	RES 270k 0402 1%	R-0402	YAGEO
40	3	R59, R61, R63	RES 10k 0402 1%	R-0402	YAGEO
41	1	R65	RES 10k 0603 1%	R-0603	YAGEO
42	1	R66	RES 200R 1206 1%	R-1206	YAGEO
43	1	R72	RES 22k 0603 1%	R-0603	YAGEO
44	2	RS3, RS4	RES 5mR 1206 1%	R-1206	SART
45	1	TYPEA	MUSB09-01-151	TYPEA connector	MATRIX
46	1	TYPEC	MUSB12-01-216	TYPEC connector	MATRIX
47	1	U1	SC8815QDER	QFN-32 4x4	SOUTHCHIP
48	1	U2	AP43781	QFN-24 4x4	Diodes Incorporated (Diodes)
49	1	U3	PI4IOE5V9554	TSSOP-16(L)	Diodes
50	1	U4	AP63205QWU-7	TSOT26	Diodes
51	1	U5	AP2120N-3.3TRG1	SOT-23	Diodes
52	1	U6	PI3DPX1207CZHEX	TQFN-42 3.5x9	Diodes
53	1	U7	PI3USB31531ZLCEX	TQFN-40 3x6	Diodes
54	1	D1	SD103AWS	SOD323	Diodes
55	1	LED - GREEN	LS-2012-02UPGC	LED-0805	

Table 1. BOM List of the CLM EVB

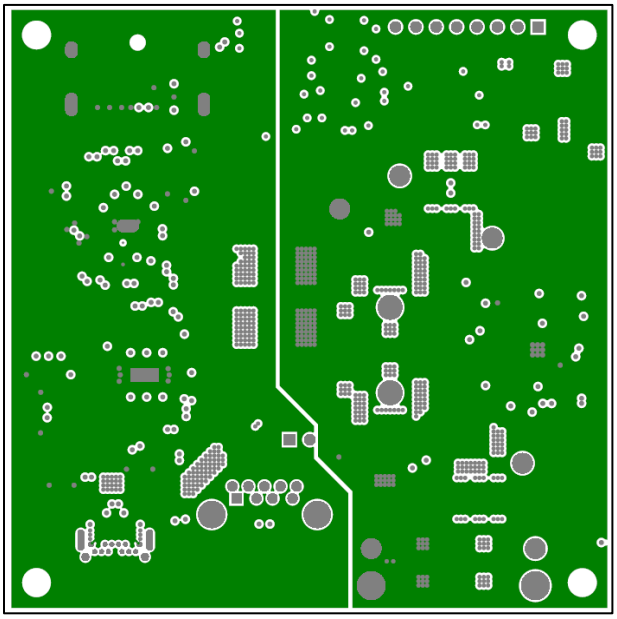
2.5 PCB Layout



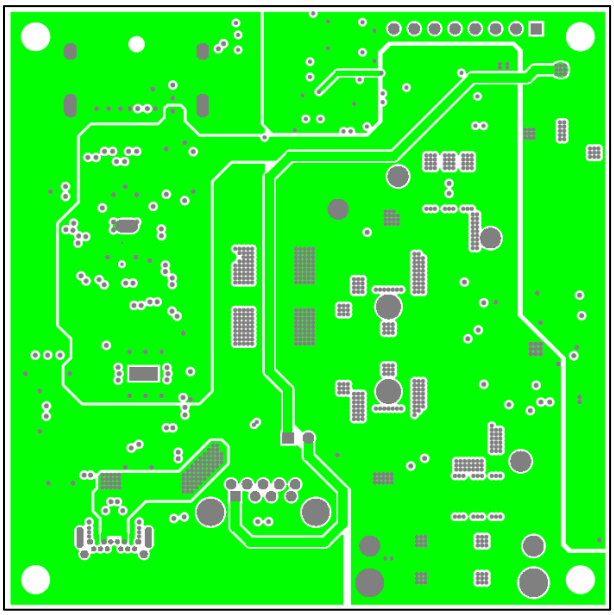
Top Layer



Bottom Layer



Single Layer 1



Single Layer 2

Chapter 3. The Charging Port Test Setups and Test Summary

3.1 USB-C PD Charging Test Setups

A Power-Z voltage tester, along with a setup board to emulate the power request for 100W (20V@5A), is shown in Figure 7. Figure 8 shows successful voltage switching stepping various fixed PDO (5V, 9V, 15V, 20V).

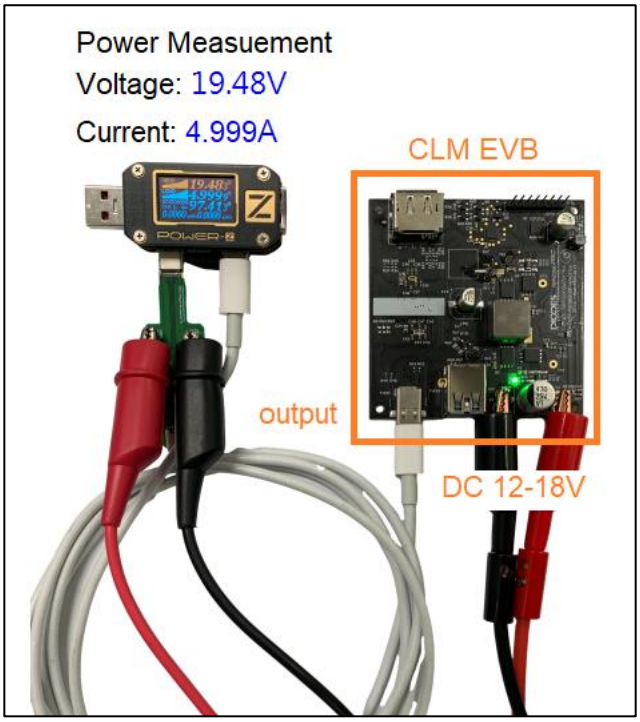


Figure 7. PD Source Charging Set-Up for 100W Output

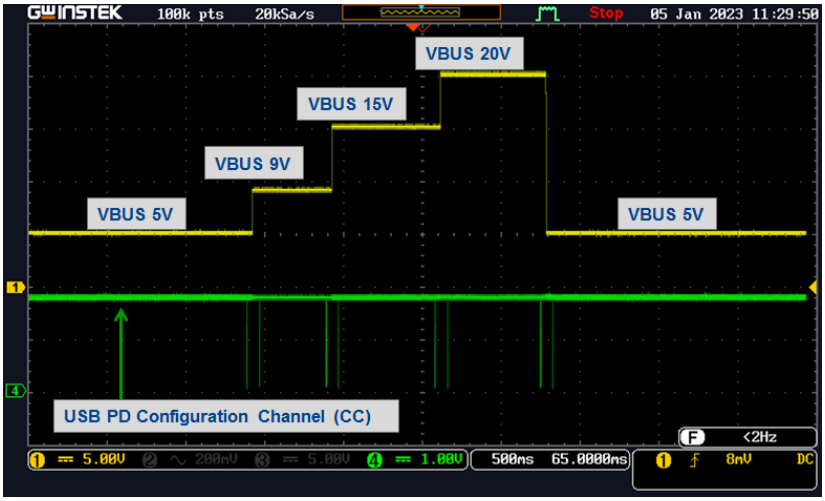


Figure 8. PD Voltage Switching Waveform vs. different PDO request

3.2 Charging Efficiency Testing

Vin	Iin	Pi	Vout	Iout	Po	Eff	Q3	Q4	Q5	Q6	L1
(V)	(A)	(W)	(V)	(A)	(W)	(%)	(℃)	(℃)	(℃)	(℃)	(℃)
12	1.336	16.04	5.06	3	15.18	94.64%	35.1	35.6	34.6	35.5	31.9
12	2.34	28.16	9.08	3	27.24	96.73%	36.9	35.4	35	35.2	32.7
12	3.914	46.96	15.11	3	45.33	96.53%	36.5	38.4	35.8	40.1	33.9
12	8.83	105.6	20.05	5	100.25	94.93%	71.5	76.2	67.3	82.6	70.6
15	1.078	16.16	5.06	3	15.18	93.94%	39.4	37	37.9	36.8	34.1
15	1.888	28.34	9.08	3	27.24	96.12%	39.1	37.2	40.2	36.5	35.3
15	3.142	47.04	15.11	3	45.33	96.36%	46.5	40.2	39.1	40.7	36.1
15	6.98	104.7	20.14	5	100.7	96.18%	56.8	63.9	54.4	66.2	57.7
18	0.906	16.3	5.07	3	15.21	93.31%	41.8	38.4	39.1	38.2	36.4
18	1.586	28.54	9.08	3	27.24	95.44%	40.8	38.5	39.1	37.9	35.2
18	2.588	46.58	15.11	3	45.33	97.32%	42.4	38.8	38.8	38.1	34.5
18	5.784	104.1	20.13	5	100.65	96.69%	51.3	52.2	50.9	58.9	46.7
20	0.82	16.4	5.07	3	15.21	92.74%	41.7	38.9	38.7	38.1	34.7
20	1.434	28.7	9.08	3	27.24	94.91%	43.8	41.4	40.8	40.9	40.5
20	2.338	46.74	15.11	3	45.33	96.98%	44.1	39.9	40.7	40.3	37.8
20	5.238	104.78	20.13	5	100.65	96.06%	68.8	56.5	54.2	58.9	47.3

Table 2. Efficiency and Thermal Test for PD Output

Vin	Vo	Io	Ripple ΔV	Ripple
(V)	(V)	(A)	(mV)	(%)
12	5	3	61	1.22%
12	9	3	57	0.63%
12	15	3	112	0.75%
12	20	5	329	1.65%
15	5	3	73	1.46%
15	9	3	82	0.91%
15	15	3	84	0.56%
15	20	5	234	1.17%
18	5	3	73	1.46%
18	9	3	92	1.02%
18	15	3	62	0.41%
18	20	5	126	0.63%
20	5	3	70	1.40%
20	9	3	101	1.12%
20	15	3	91	0.61%
20	20	5	120	0.60%

Table 3. Output Ripple during PD Voltage Switching

Vin	PDO	Vout	Iout	VBUS			
(V)	(V)	(V)	(A)	Overshoot(V)	Tolerance (%)	Undershoot(V)	Tolerance (%)
12	5	5.06	0.5<-->2.5	5.36	5.93	4.7	-7.11
12	9	9.08	0.5<-->2.5	9.4	3.52	8.72	-3.96
12	15	15.11	0.5<-->2.5	15.6	3.24	14.6	-3.38
12	20	20.12	0.5<-->4.5	21.24	5.57	18.8	-6.56
15	5	5.06	0.5<-->2.5	5.38	6.32	4.72	-6.72
15	9	9.08	0.5<-->2.5	9.4	3.52	8.68	-4.41
15	15	15.11	0.5<-->2.5	15.52	2.71	14.68	-2.85
15	20	20.12	0.5<-->4.5	21.04	4.57	19.2	-4.57
18	5	5.06	0.5<-->2.5	5.38	6.32	4.72	-6.72
18	9	9.08	0.5<-->2.5	9.4	3.52	8.6	-5.29
18	15	15.1	0.5<-->2.5	15.52	2.78	14.68	-2.78
18	20	20.14	0.5<-->4.5	20.84	3.48	19.32	-4.07
20	5	5.07	0.5<-->2.5	5.36	5.72	4.72	-6.90
20	9	9.08	0.5<-->2.5	9.4	3.52	8.6	-5.29
20	15	15.1	0.5<-->2.5	15.48	2.52	14.68	-2.78
20	20	20.12	0.5<-->4.5	20.88	3.78	19.24	-4.37

Table 4. Dynamic Loading for Various Fixed PDO Output

Vin	Vo	Io	Rising	Overshoot	Overshoot	Vin	Vo	Io	Falling	Undershoot	Undershoot
(V)	(V)	(A)	(ms)	(V)	(%)	(V)	(V)	(A)	(ms)	(V)	(%)
12	5-->9	3	1.86	9.28	3.1%	12	9-->5	3	0.54	4.68	-6.4%
12	9-->15	3	2.66	15.36	2.4%	12	15-->9	3	0.78	8.72	-3.1%
12	15-->20	3	0.68	20.68	3.4%	12	20-->15	3	0.64	14.68	-2.1%
15	5-->9	3	1.78	9.28	3.1%	15	9-->5	3	0.54	4.64	-7.2%
15	9-->15	3	2.7	15.36	2.4%	15	15-->9	3	0.78	8.68	-3.6%
15	15-->20	3	0.64	20.52	2.6%	15	20-->15	3	0.54	14.68	-2.1%
18	5-->9	3	1.78	9.28	3.1%	18	9-->5	3	0.54	4.68	-6.4%
18	9-->15	3	2.66	15.36	2.4%	18	15-->9	3	0.7	8.64	-4.0%
18	15-->20	3	0.64	20.52	2.6%	18	20-->15	3	0.66	14.72	-1.9%
20	5-->9	3	1.8	9.28	3.1%	20	9-->5	3	0.56	4.72	-5.6%
20	9-->15	3	2.66	15.32	2.1%	20	15-->9	3	0.78	8.68	-3.6%
20	15-->20	3	0.56	20.56	2.8%	20	20-->15	3	0.68	14.72	-1.9%

Table 5. Dynamic Performance of Voltage Switching

Vin	Iin	Standby Power
(V)	(mA)	(mW)
12	1.40	16.8
15	1.41	21.2
18	1.43	25.7
20	1.46	29.2

Table 6. Standby Power Consumption without IO Expander

Chapter 4. UFP Video/Data Setups and Test Summary

4.1 UFP Video/Data Setups

Figure 9 shows the connection setup to validate the UFP video path from a notebook (MacBook Pro in this example) to DP Monitor (HP Monitor) through the CLM EVB. A USB-C to USB-C cable connects between USB-C Port of MacBook Pro and USB-C port of the CLM EVB.

This video test confirms that the CLM EVB can support DP with Pin Assignment C/D.

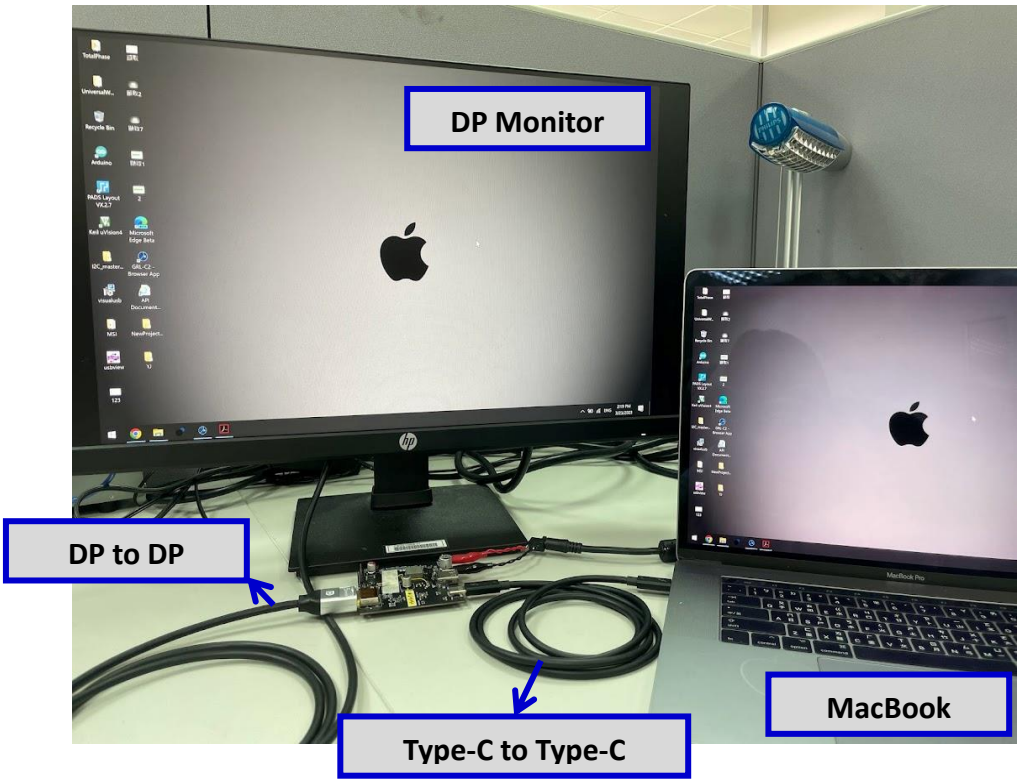


Figure 9. UFP Test Setups for Notebook to DP Monitor

Figure 10 shows the connection setup to validate the UFP video path from a smartphone (Galaxy Note10 in this example) to DP Monitor (HP Monitor) through the CLM EVB. A USB-C to USB-C cable connects between USB-C Port Smartphone and USB-C port of the CLM EVB.

This video test confirms that the CLM EVB supports DP with Pin Assignment C/D.

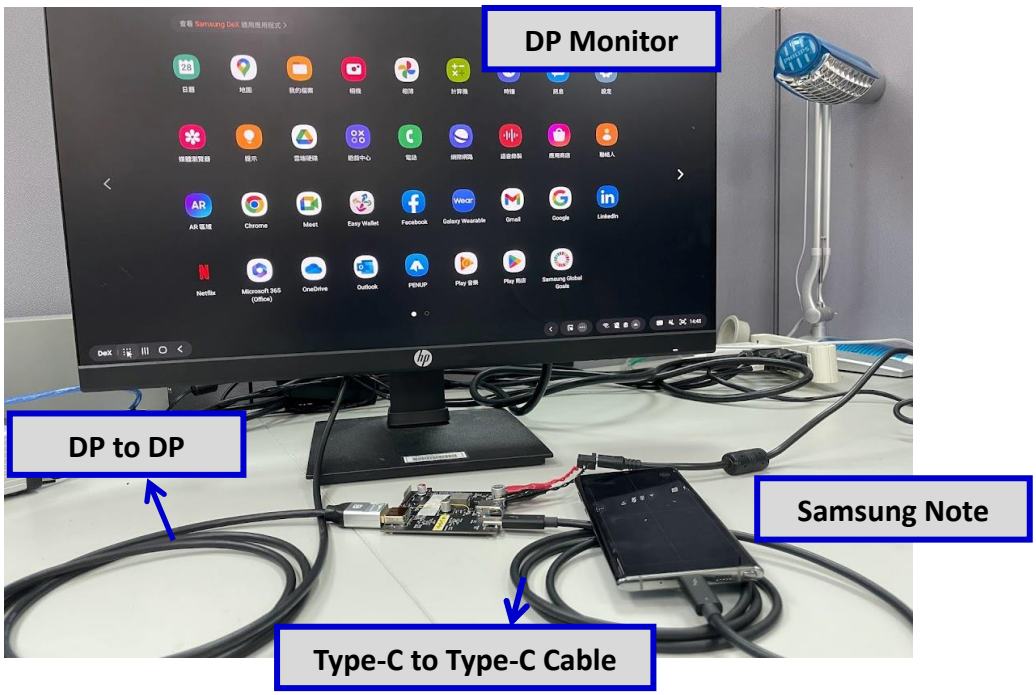


Figure 10. UFP Test Setups for Smartphone to DP Monitor

Figure 11 shows the connection setup to validate the UFP video path from a Desktop PC (HP Desktop in this example) to DP Monitor (HP Monitor) through the CLM EVB. A DP to DP cable connects between DP connector of CLM EVB and DP Monitor input port, and a USB-C to USB-C cable connects between USB-C Port of Desktop PC and USB-C port of the CLM EVB.

This video test confirms the CLM EVB can support DP with Pin Assignment E.

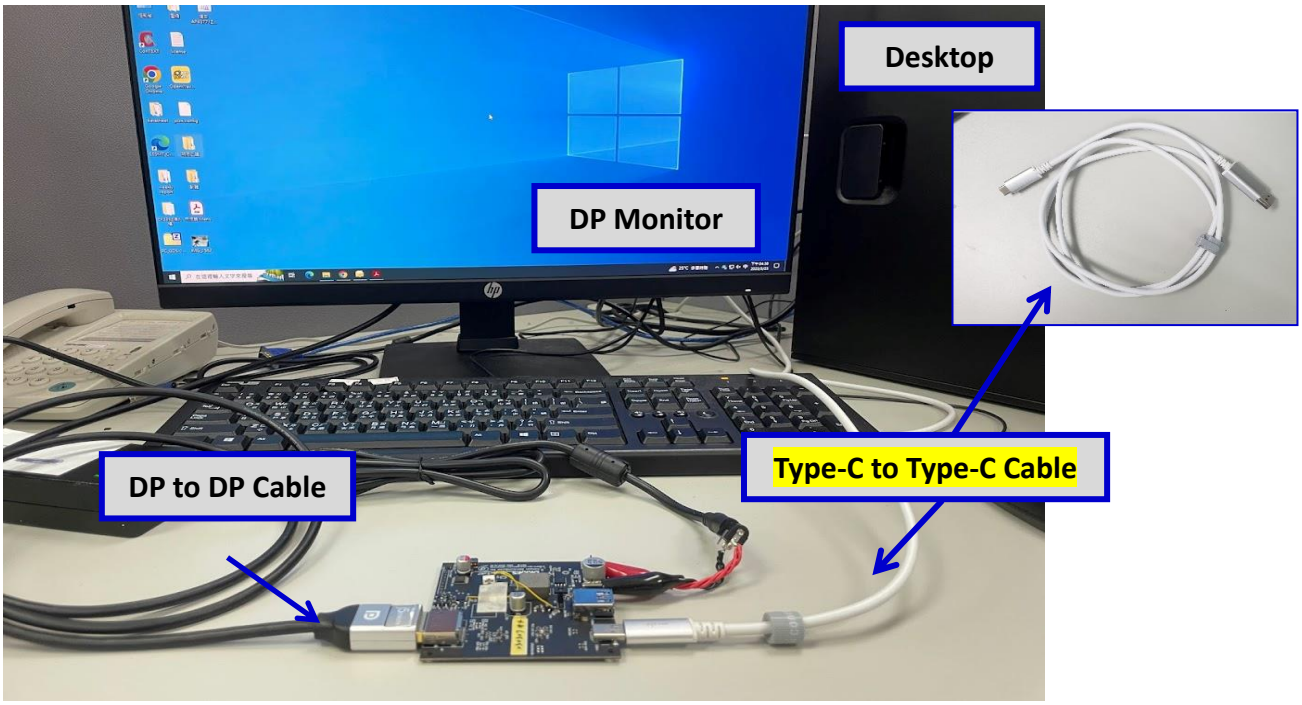
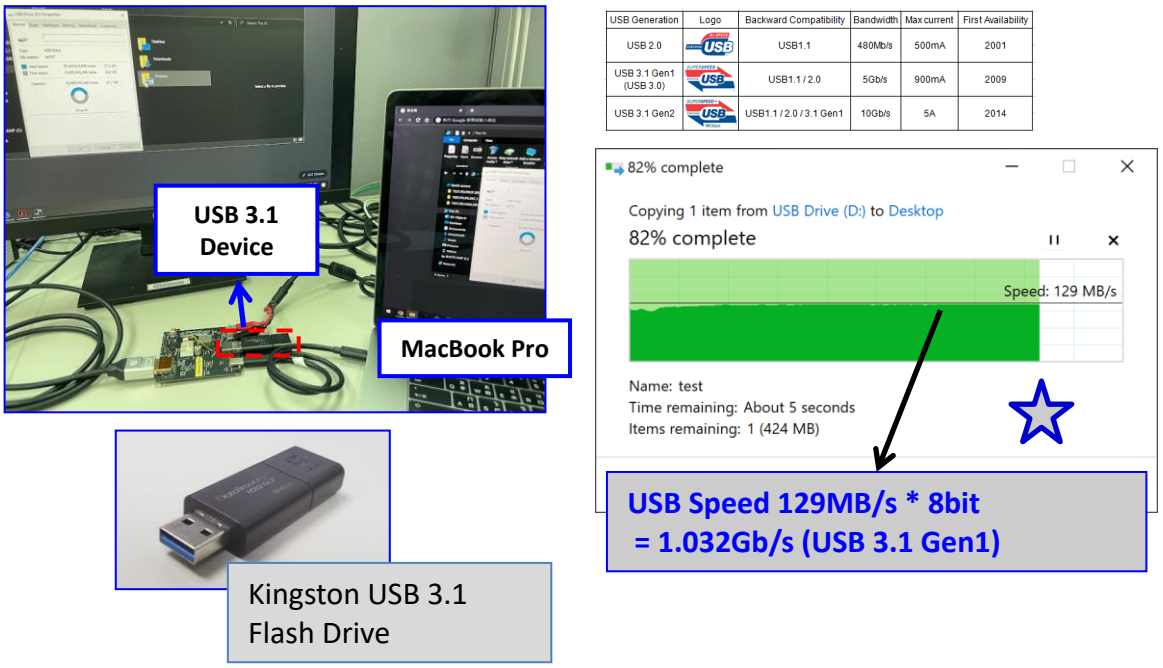


Figure 11. UFP Test Setups for Desktop PC to DP Monitor

Device	USB-C flip / non-flip	Pin assignment request	Data Role swap	Power request
MacBook Air(2019) + USB-C Cable	OK	C / D	OK	20V/5A
MacBook (2016) + USB-C Cable	OK	Depending on MacBook Selection (C or D)	OK	20/5A
MacBook Pro(2017 A1707) + USB-C Cable	OK	D	OK	20V/5A
MacBookAir(2022 A2337) + USB-C Cable	OK		OK	20V/5A
MacBookAir(2020 A2179) + USB-C Cable	OK		OK	20V/5A
MacBookPro(2021 A2442) + USB-C Cable	OK		OK	20V/5A
MacBookPro(2023 A2779) + USB-C Cable	OK		OK	20V/5A
MacBookPro(inter2020 A2289) + USB-C Cable	OK		OK	20V/3A
MakBookPro(2021 A2485) + USB-C Cable	OK		OK	20/5A
Lenovo ThinkPad E14 Gen2(2020)+ USB-C Cable	OK		OK	20V/3.25A
Lenovo ThinkPad X1 Carbon Gen 8(2020)+ USB-C Cable	OK		OK	20V/3.25A
Lenovo Legion Y540-15IRH-PG0(2020)+ USB-C Cable	OK		OK	5V/3A
Lenovo Yoga Slim 7i Pro(2021)+ USB-C Cable	OK		OK	20V/5A
DELL Inspiron 16 5625-R1508STW(2022)+ USB-C Cable	OK		OK	20V/3A
DELL XPS13-9310-P3708STW(2020)+ USB-C Cable	OK		OK	20V/2.25A
DELL G15-5525(2021)+ USB-C Cable	OK		OK	5V/3A
ASUS ZenBook 13 OLED UX325UA(2020)+ USB-C Cable	OK		OK	20V/3A
ASUS ROG Zephyrus G14(2022)+ USB-C Cable	OK		OK	20V/5A
HP ProBook (2021 AX201NGW)	OK		OK	20V/5A
HP EliteBook 640 14 inch G9 Notebook PC(2022)+ USB-C Cable	OK		OK	20V/5A
iPad Pro (III A2377)	OK	D	OK	20V/4.4A
iPad pro III (12.9 inch)	OK	D	OK	
iPhone 15 / Plus	OK	D	OK	
Samsung Galaxy S20 + USB-C Cable	OK	C	OK	5V/3A
Samsung Galaxy S21 / S22 + USB-C Cable	OK	D	OK	9V/3A
Samsung NOTE 10 / Plus+ USB-C Cable	OK	C / D	OK	5V/3A
HUAWEI P60	OK	C	OK	9V/5A
HUAWEI P30 Pro / Mate 20	OK	C	OK	5V/2A
Microsoft Surface GO 3 (Mode I 1901, Win 11 version 21H2)	OK	D	OK	20V/2.25A
Desktop PC + CableCreation CD0738-G (DP-to-USB-C Cable)	OK	C (Non-Standard-Compliance Cable)	OK	5V/3A (no E-mark)
Desktop PC + Moshi 5K (DP-to-USB-C Cable)	OK	E (Standard-Compliance Cable)	OK	5V/3A (no E-mark)
Nintendo Switch 2019/2021	OK	C	OK	15V/3A

Table 7. Pin Assignment Compliance Test Summary

Figure 12 shows the connection setup to USB 3.1 functionality and speed (USB 3.1 Gen1) path from a notebook (MacBook Pro in this example) to USB Type-A through the CLM EVB. A USB-C-to-USB-C cable connects between USB-C Port of MacBook Pro and USB-C port of the CLM EVB.



USB Generation	Logo	Backward Compatibility	Bandwidth	Max current	First Availability
USB 2.0		USB1.1	480Mb/s	500mA	2001
USB 3.1 Gen1 (USB 3.0)		USB1.1 / 2.0	5Gb/s	900mA	2009
USB 3.1 Gen2		USB1.1 / 2.0 / 3.1 Gen1	10Gb/s	5A	2014

Figure 12. USB 3.1 Gen 1 /Gen 2 Test Setups

4.2 Signal Integrity (Eye Diagram) Test

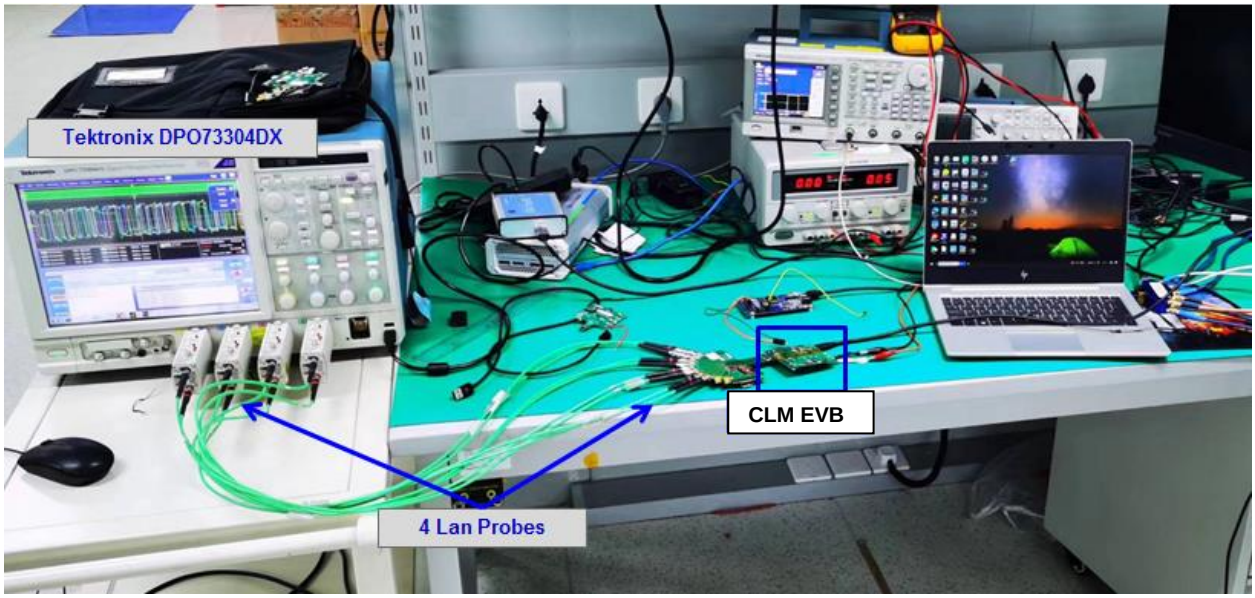


Figure 13. Eye Diagram Test Setups

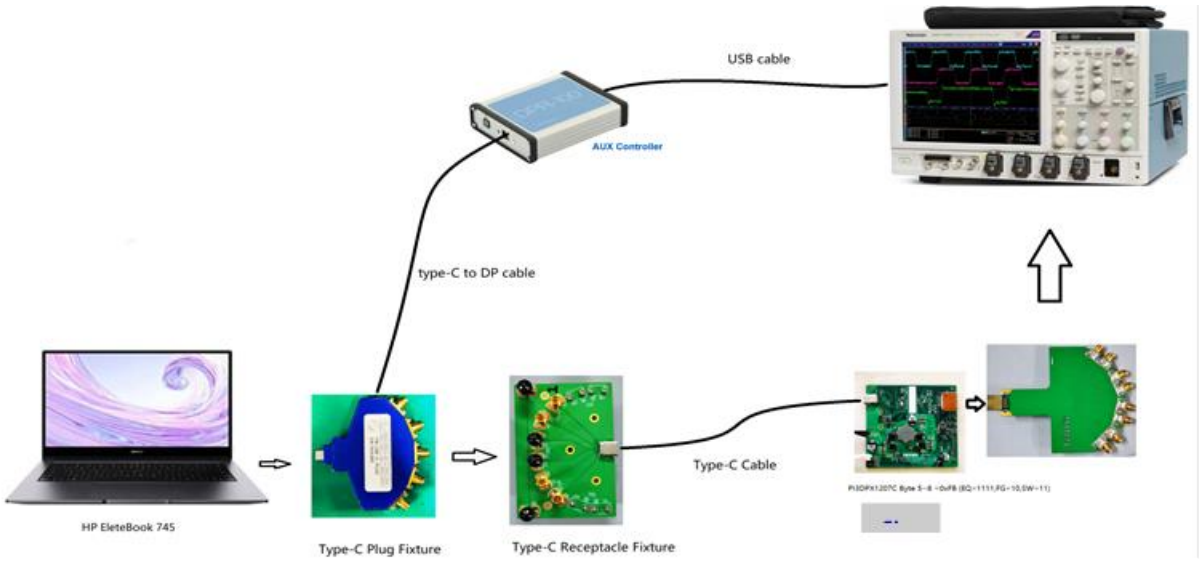


Figure 14. Eye Diagram Test Setups for CLM EVB

TekExpress Automated Test Solution
TekExpress DisplayPort

Setup Information			
DUT ID	CLM-PD DEMO BOARD	Scope Model	DPO73304DX
Date/Time	2023-01-03 15:56:30	Scope Serial Number	B280031
Device Type	DisplayPort	SPC, FactoryCalibration	PASS;PASS
App Version	Display Port:10.3.5.4	Scope F/W Version	10.8.7 Build 29
TekExpress Version	Framework:4.9.0.5	DPOJET Version	10.3.0.5
Execution Mode	Live	ProbeCH1 Model	P7313SMA
Overall Compliance Mode	Yes	ProbeCH1 Serial Number	B021953
OverallResult	Pass	ProbeCH2 Model	P7313SMA
Overall Execution Time	0:34:42	ProbeCH2 Serial Number	B021949
DUT Automation Method	DPR-100	ProbeCH3 Model	P7313SMA
Connector	Standard	ProbeCH3 Serial Number	B020655
CTS Version	CTS 1.4	ProbeCH4 Model	P7313SMA
DPR100 Version	DP Rev 1.2	ProbeCH4 Serial Number	B022534
DUT COMMENT:	General Comment - DisplayPort		

Test Name Summary Table	
Test 3.1_Eye diagram testing	Pass
Total Measurements Executed : 72 : Pass = 72 : Fail = 0 : Skipped = 0 : Error = 0	

Test 3.1_Eye diagram testing

Lane	Measurement Details	Measured Value	Units	Test Result	Margin	Low Limit	High Limit
Lane0	MaskHits TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane0	Width TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	0.6357	UI	Pass	0.2157	0.42	N.A
Lane0	Height TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	387.1891	mV	Pass	322.1891	65	N.A
Lane0	MaskHits TP3_EQ1-Worst Case-CTLE -5dB:HBR3 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane0	Width TP3_EQ1-Worst Case-CTLE -5dB:HBR3 NoSSC 0dB 800mV Run 1	0.6159	UI	Pass	0.1959	0.42	N.A
Lane0	Height TP3_EQ1-Worst Case-CTLE -5dB:HBR3 NoSSC 0dB 800mV Run 1	96.8047	mV	Pass	31.8047	65	N.A
Lane1	MaskHits TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane1	Width TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	0.6735	UI	Pass	0.2535	0.42	N.A
Lane1	Height TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	398.4142	mV	Pass	333.4142	65	N.A
Lane1	MaskHits TP3_EQ1-Worst Case-CTLE -6dB:HBR3 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane1	Width TP3_EQ1-Worst Case-CTLE -6dB:HBR3 NoSSC 0dB 800mV Run 1	0.6010	UI	Pass	0.1810	0.42	N.A
Lane1	Height TP3_EQ1-Worst Case-CTLE -6dB:HBR3 NoSSC 0dB 800mV Run 1	99.0293	mV	Pass	34.0293	65	N.A

Lane2	MaskHits TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane2	Width TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	0.6651	UI	Pass	0.2451	0.42	N.A
Lane2	Height TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	454.2098	mV	Pass	389.2098	65	N.A
Lane2	MaskHits TP3_EQ1-Worst Case-CTLE -6dB:HBR3 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane2	Width TP3_EQ1-Worst Case-CTLE -6dB:HBR3 NoSSC 0dB 800mV Run 1	0.6136	UI	Pass	0.1936	0.42	N.A
Lane2	Height TP3_EQ1-Worst Case-CTLE -6dB:HBR3 NoSSC 0dB 800mV Run 1	118.9819	mV	Pass	53.9819	65	N.A
Lane3	MaskHits TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane3	Width TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	0.6847	UI	Pass	0.2647	0.42	N.A
Lane3	Height TP3_EQ1-Zero Length-CTLE 0dB:HBR3 NoSSC 0dB 800mV Run 1	430.5102	mV	Pass	365.5102	65	N.A
Lane3	MaskHits TP3_EQ1-Worst Case-CTLE -7dB:HBR3 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane3	Width TP3_EQ1-Worst Case-CTLE -7dB:HBR3 NoSSC 0dB 800mV Run 1	0.5914	UI	Pass	0.1714	0.42	N.A
Lane3	Height TP3_EQ1-Worst Case-CTLE -7dB:HBR3 NoSSC 0dB 800mV Run 1	116.2218	mV	Pass	51.2218	65	N.A
Lane0	MaskHits TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane0	Width TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0.6376	UI	Pass	0.2176	0.42	N.A
Lane0	Height TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	446.1417	mV	Pass	342.1417	104	N.A
Lane0	MaskHits TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane0	Width TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0.6868	UI	Pass	0.2668	0.42	N.A
Lane0	Height TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	372.6041	mV	Pass	268.6041	104	N.A
Lane1	MaskHits TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane1	Width TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0.6942	UI	Pass	0.2742	0.42	N.A
Lane1	Height TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	446.5405	mV	Pass	342.5405	104	N.A
Lane1	MaskHits TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane1	Width TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0.7069	UI	Pass	0.2869	0.42	N.A
Lane1	Height TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	375.5491	mV	Pass	271.5491	104	N.A
Lane2	MaskHits TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane2	Width TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0.6507	UI	Pass	0.2307	0.42	N.A
Lane2	Height TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	504.6607	mV	Pass	400.6607	104	N.A
Lane2	MaskHits TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane2	Width TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0.7034	UI	Pass	0.2834	0.42	N.A

Lane2	Height TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	391.6735	mV	Pass	287.6735	104	N.A
Lane3	MaskHits TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane3	Width TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0.6917	UI	Pass	0.2717	0.42	N.A
Lane3	Height TP3_EQ1-Zero Length-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	447.7459	mV	Pass	343.7459	104	N.A
Lane3	MaskHits TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0	Hits	Pass	0.0000	N.A	0
Lane3	Width TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	0.7286	UI	Pass	0.3086	0.42	N.A
Lane3	Height TP3_EQ1-Worst Case-sdlactle:HBR2 NoSSC 0dB 800mV Run 1	393.6757	mV	Pass	289.6757	104	N.A
Lane0	MaskHits:RBR NoSSC 0dB 800mV Run1	0	Hits	Pass	0.0000	N.A	0
Lane0	Eye Width:RBR NoSSC 0dB 800mV Run1	0.8859	UI	Pass	0.1399	0.746	N.A
Lane0	Eye Height:RBR NoSSC 0dB 800mV Run1	600.1956	mV	Pass	200.1956	400	N.A
Lane0	MaskHits:HBR NoSSC 0dB 800mV Run1	0	Hits	Pass	0.0000	N.A	0
Lane0	Eye Width:HBR NoSSC 0dB 800mV Run1	0.8779	UI	Pass	0.2979	0.58	N.A
Lane0	Eye Height:HBR NoSSC 0dB 800mV Run1	587.4368	mV	Pass	237.4368	350	N.A
Lane1	MaskHits:RBR NoSSC 0dB 800mV Run1	0	Hits	Pass	0.0000	N.A	0
Lane1	Eye Width:RBR NoSSC 0dB 800mV Run1	0.8915	UI	Pass	0.1455	0.746	N.A
Lane1	Eye Height:RBR NoSSC 0dB 800mV Run1	644.2939	mV	Pass	244.2939	400	N.A
Lane1	MaskHits:HBR NoSSC 0dB 800mV Run1	0	Hits	Pass	0.0000	N.A	0
Lane1	Eye Width:HBR NoSSC 0dB 800mV Run1	0.8926	UI	Pass	0.3126	0.58	N.A
Lane1	Eye Height:HBR NoSSC 0dB 800mV Run1	623.1296	mV	Pass	273.1296	350	N.A
Lane2	MaskHits:RBR NoSSC 0dB 800mV Run1	0	Hits	Pass	0.0000	N.A	0
Lane2	Eye Width:RBR NoSSC 0dB 800mV Run1	0.8941	UI	Pass	0.1481	0.746	N.A
Lane2	Eye Height:RBR NoSSC 0dB 800mV Run1	624.2267	mV	Pass	224.2267	400	N.A
Lane2	MaskHits:HBR NoSSC 0dB 800mV Run1	0	Hits	Pass	0.0000	N.A	0
Lane2	Eye Width:HBR NoSSC 0dB 800mV Run1	0.8800	UI	Pass	0.3000	0.58	N.A
Lane2	Eye Height:HBR NoSSC 0dB 800mV Run1	608.1170	mV	Pass	258.1170	350	N.A
Lane3	MaskHits:RBR NoSSC 0dB 800mV Run1	0	Hits	Pass	0.0000	N.A	0
Lane3	Eye Width:RBR NoSSC 0dB 800mV Run1	0.9044	UI	Pass	0.1584	0.746	N.A
Lane3	Eye Height:RBR NoSSC 0dB 800mV Run1	622.4479	mV	Pass	222.4479	400	N.A
Lane3	MaskHits:HBR NoSSC 0dB 800mV Run1	0	Hits	Pass	0.0000	N.A	0
Lane3	Eye Width:HBR NoSSC 0dB 800mV Run1	0.9039	UI	Pass	0.3239	0.58	N.A
Lane3	Eye Height:HBR NoSSC 0dB 800mV Run1	584.8412	mV	Pass	234.8412	350	N.A
COMMENTS	DFE Taps: 1, Amplitude: 0.05V, Threshold: 0						

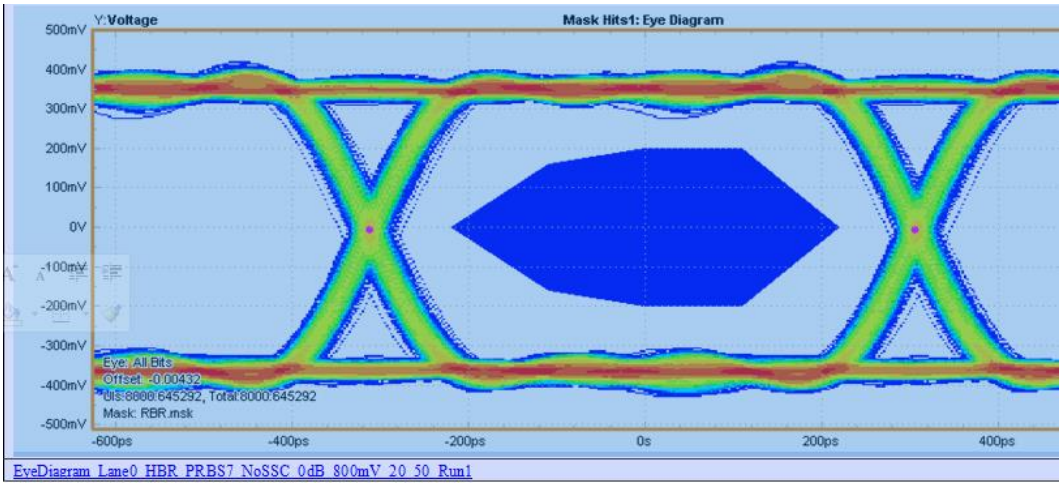


Figure 15. Eye Diagram in CLM EVB

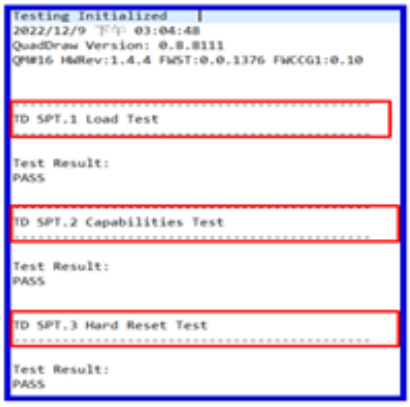
Chapter 5. USB-C PD Protocol Compliance Test

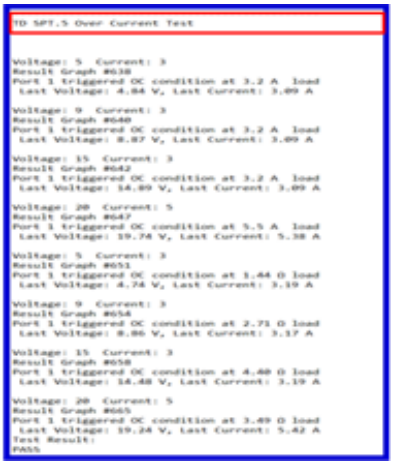
5.1 Ellisys

Ellisys USB Compliance Report

Date and time	Thursday, 19 October 2023 16:51:57 GMT+8
Vendor	Diodes
Product	AP43781_100W
Product revision	AP43781
Test ID	0
Component Under Test	1
Port Label	1
Generator used	Ellisys USB Explorer 350 (EX350-62136)
Analyzer used	Ellisys USB Explorer 350 (EX350-62138)
Software version	Report generated with version 3.1.8686
Overall result	**Passed**

5.2 Quadramax





5.3 LeCroy

Teledyne LeCroy
USB Compliance F

Chapter 6. Reference Documents

6.1 AP43781 Datasheet

Please refer to: https://www.diodes.com/assets/Datasheets/AP43781.pdf

6.2 PI3DPX1207 Datasheet

Please refer to: https://www.diodes.com/assets/Databriefs/PI3DPX1207C-Product-Brief.pdf

6.3 PI3USB31531 Datasheet

Please refer to: https://www.diodes.com/assets/Databriefs/PI3USB31531.pdf

6.4 PI4IOE5V9554 Datasheet

Please refer to: https://www.diodes.com/assets/Datasheets/PI4IOE5V9554-PI4IOE5V9554A.pdf

Chapter 7. Revision History

Item NO	Hardware Version	Firmware Version	Change Description	Date
1	1.0	1.0	1st Release	2023/10/18
2	1.0	1.1	update firmware udpate Table7. Pin Assignment Compliance Test Summary	2024/2/7

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