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Chapter 1 Summary

1.1 General Description

The 65W ACF PD3.0 PPS Evaluation Board is composed of three main controllers, AP3306, APR340 and AP43771V. AP3306 is a highly integrated Active Clamp Flyback (ACF) controller that is optimally designed for offline power supply to meet ultra-low standby power, high power density, and comprehensive protection requirements. The APR340 is a secondary side Synchronous Rectification (SR) Controller. The AP43771V, a protocol decoder in charge of matching the associated charger capacity and request by an attached Type C-equipped device under charged (DUC), regulates the feedback network of the charger to fulfill voltage and current requirements from DUC. In addition, Gallium Nitride (GaN) FET is employed to further improve the efficiency and thermal performance.

1.2 Key Features

1.2.1 System Key Features

- Diodes Patented ACF Topology Implementation for Critical Efficiency Improvement Approaches
- Cost-Effective Implementation for High Efficiency High Power Density Charger
- High-Voltage Startup low standby power (<20mW)
- Meets DOE VI and COC Tier 2 Efficiency Requirements
- USB Type-C Port - Support the Maximum Output of 65W PD3 Function and PPS 21V@20mV/step
- SSR Topology Implementation with an Opto-coupler for Accurate Step Voltage Controlling
- Low overall system BOM cost

1.2.2 AP3306 Key Features

- Active Clamp Flyback Topology with Recycled Leakage Energy and Zero Voltage Switching Functions
- High-Voltage Startup
- Embedded VCC LDO for VCCL pin to Guarantee Wide Range Output Voltage
- Constant, Low Output Current in Output Short Situation
- Non-Audible-Noise Quasi-Resonant Control
- Soft Start During Startup Process
- Frequency Fold Back for High Average Efficiency
- Secondary Winding Short Protection with FOCP
- Frequency Dithering for Reducing EMI
- X-CAP Discharge Function
- Useful Pin fault protection:
  SENSE Pin Floating Protection/
  FB/Opto-Coupler Open/Short Protection
- Comprehensive System Protection Feature:
  VOVP/OLP/BNO/SOVP/SUVP

1.2.3 APR340 Key Features

- Synchronous Rectification Works with DCM / QR / ACF operation modes
- Eliminate Resonant Ringing Interference
- Fewest External Components used

1.2.4 AP43771V Key Feature

- Support USB PD Rev 3.0 V1.2
- USB-IF PD3.0/PPS Certified TID 4312
- Qualcomm QC5 Certified: QC20201127203
- MTP for System Configuration
- OTP for Main Firmware
- Operating Voltage Range: 3.3V to 21V
- Built-In Regulator for CV and CC Control
- Programmable OVP/UVP/OCP/OTP
- Support Power Saving Mode
- External N -MOSFET Control for VBUS Power Delivery
- Support e-Marker Cable Detection
- QFN-24Q

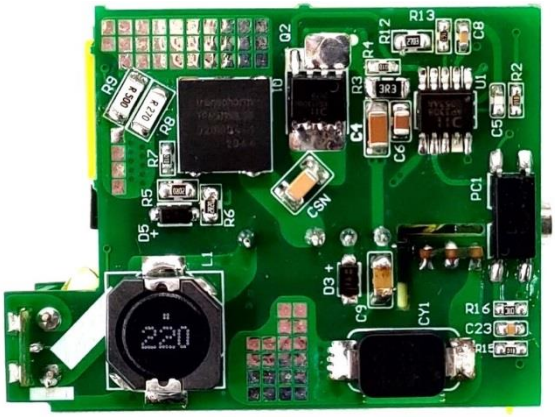
1.3 Applications

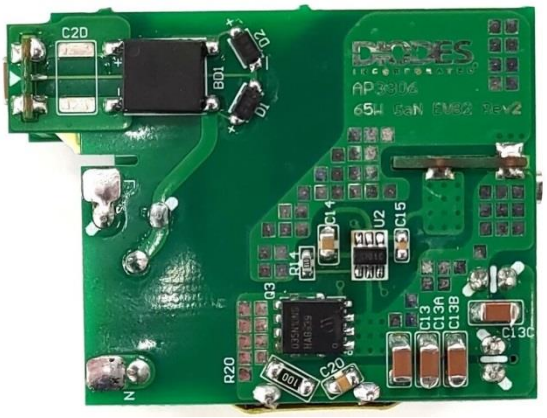
- Quick Charger with full power range of PD3.0 PPS

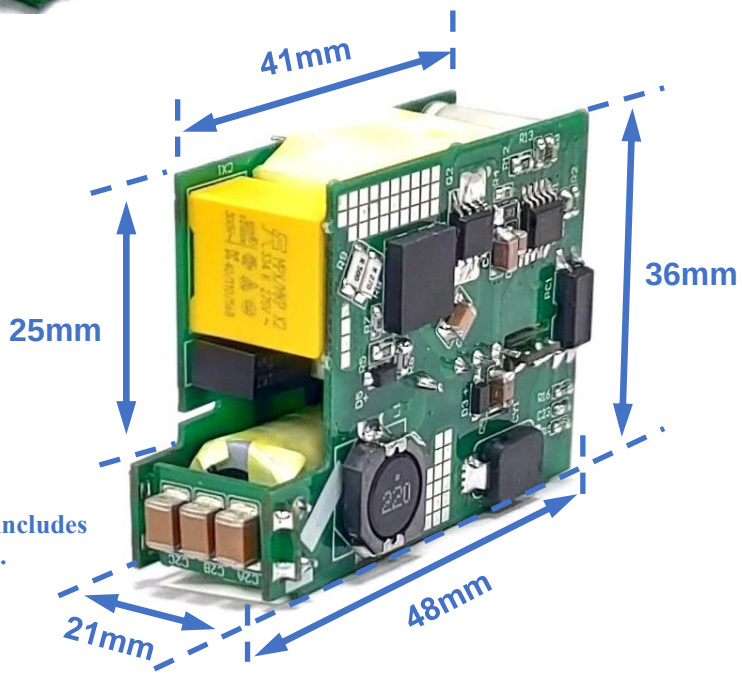
1.4 Main Power Specifications

Parameter	Value
Input Voltage	$90V_{AC}$ to $264V_{AC}$
Input standby power	< 30mW
Main Output (Vo / Io)	PDO: 5V/3A, 9V/3A, 15V/3A, 20V/3.25A,
	APDO: 3.3V to 21V/3A
Voltage Step	PPS 20mV step voltage, 3.3V-21V
Efficiency	Comply with CoC version 5 tier-2
Total Output Power	65W (at PDO 20V/3.25A)
Protections	OCP, OVP, UVP, OLP, OTP, SCP
Dimensions	PCB: 36 * 48 * 21 mm^3, 1.417" * 1.89" * 0.827" $inch^3$ Case: 40 * 52 * 25 mm^3, 52CC, 3.17 CI
Power Density Index	1.25 W/CC; 20.48 W/CI

1.5 Evaluation Board Pictures







The dimension "21mm" includes the height of components.

Chapter 2 Power Supply Specification

2.1 Specification and Test Results

Parameter	Value	Test Summary
Input Voltage / Frequency	90V_{AC} to 264V_{AC} / 50Hz or 60Hz	Test Condition
Input Current	<2A_{RMS}	
Standby Power	< 30mW, load disconnected	**PASS,** 18.3mW@230V_{AC}/50Hz
5V/3A Average Efficiency	CoC Version 5, Tier-2 Efficiency >81.84%	**PASS,** 91.08@115VAC/60Hz 90.68@230VAC/50Hz
5V/0.3A Efficiency (10% Load)	CoC Version 5, Tier2 Efficiency >72.48%	**PASS,** 88.24@115VAC/60Hz 87.95@230VAC/50Hz
9V/3A Average Efficiency	CoC Version 5,Tier2 Efficiency >87.30%	**PASS,** 92.92@115VAC/60Hz 92.92@230VAC/50Hz
9V/0.3A Efficiency (10% Load)	CoC Version 5,Tier2 Efficiency >77.30%	**PASS,** 88.22@115VAC/60Hz 89.46@230VAC/50Hz
15V/3A Average Efficiency	CoC Version 5,Tier2 Efficiency >88.85%	**PASS,** 93.51@115VAC/60Hz 93.68@230VAC/50Hz
15V/0.3A Efficiency (10% Load)	CoC Version 5,Tier2 Efficiency >78.85%	**PASS,** 90.79@115VAC/60Hz 93.85@230VAC/50Hz
20V/3.25A Average Efficiency	CoC Version 5,Tier2 Efficiency >89%	**PASS,** 93.55@115VAC/60Hz 93.41@230VAC/50Hz
20V/0.325A Efficiency (10% Load)	CoC Version 5,Tier2 Efficiency >79%	**PASS,** 91.06@115VAC/60Hz 89.43@230VAC/50Hz
Output Voltage Regulation Tolerance	+/- 5%	**PASS,**
16V PPS	3.3V – 16V +/- 5%, 0~2.8A +/-150mA	**PASS,**
21V PPS	3.3V – 21V +/- 5%, 0~2.1A +/-150mA	**PASS,**
Conducted EMI	>5dB Margin; according to EN55032 Class B	

2.2 Compliance

Parameter	Test conditions	Low to High	High to Low	standard	Test Summary
Output Voltage Transition time	5V/3A to 9V/3A, 90Vac/60Hz	55.02ms	53.94ms	275ms <	Pass
	5V/3A to 9V/3A, 264Vac/50Hz	52.88ms	52.70ms		Pass
	9V/3A to 15V/3A, 90Vac/60Hz	74.56ms	74.10ms		Pass
	9V/3A to 15V/3A, 2640Vac/50Hz	73.33ms	76.70ms		Pass
	15V/3A to 20V/3A, 90Vac/60Hz	60.99ms	61.62ms		Pass
	15V/3A to 20V/3A, 264Vac/50Hz	61.60ms	60.69ms		Pass
Output Connector	USB Type-C *1-				
Temperature	90Vac , Full Load				
Dimensions (W /D/ H)	L36mm x48mm x 21mm (with foldable AC pin)				

Chapter 3 Schematic

3.1 Board Schematic

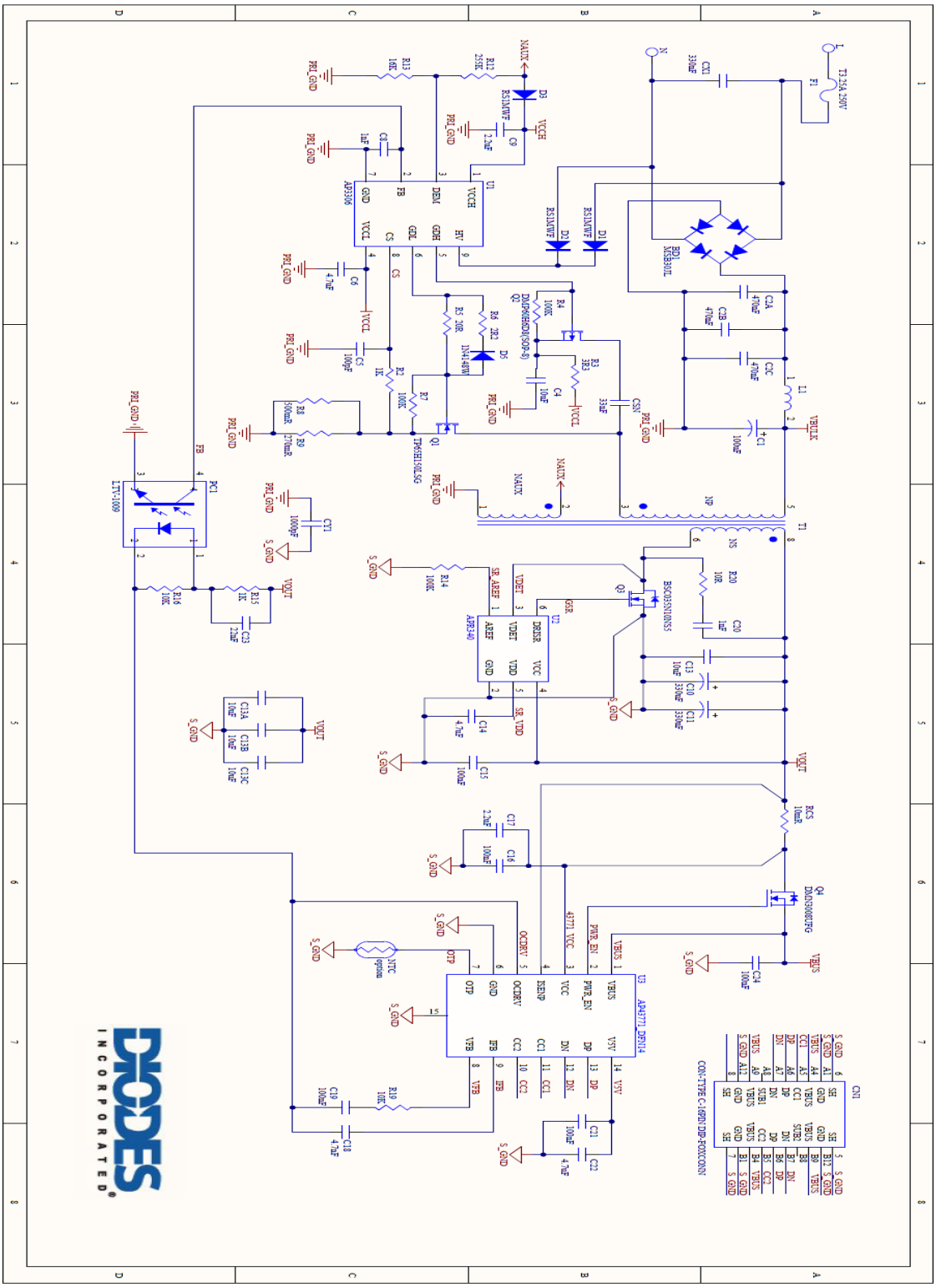


Figure 3: 65W PD3.0 PPS Adapter EVB2 Schematic

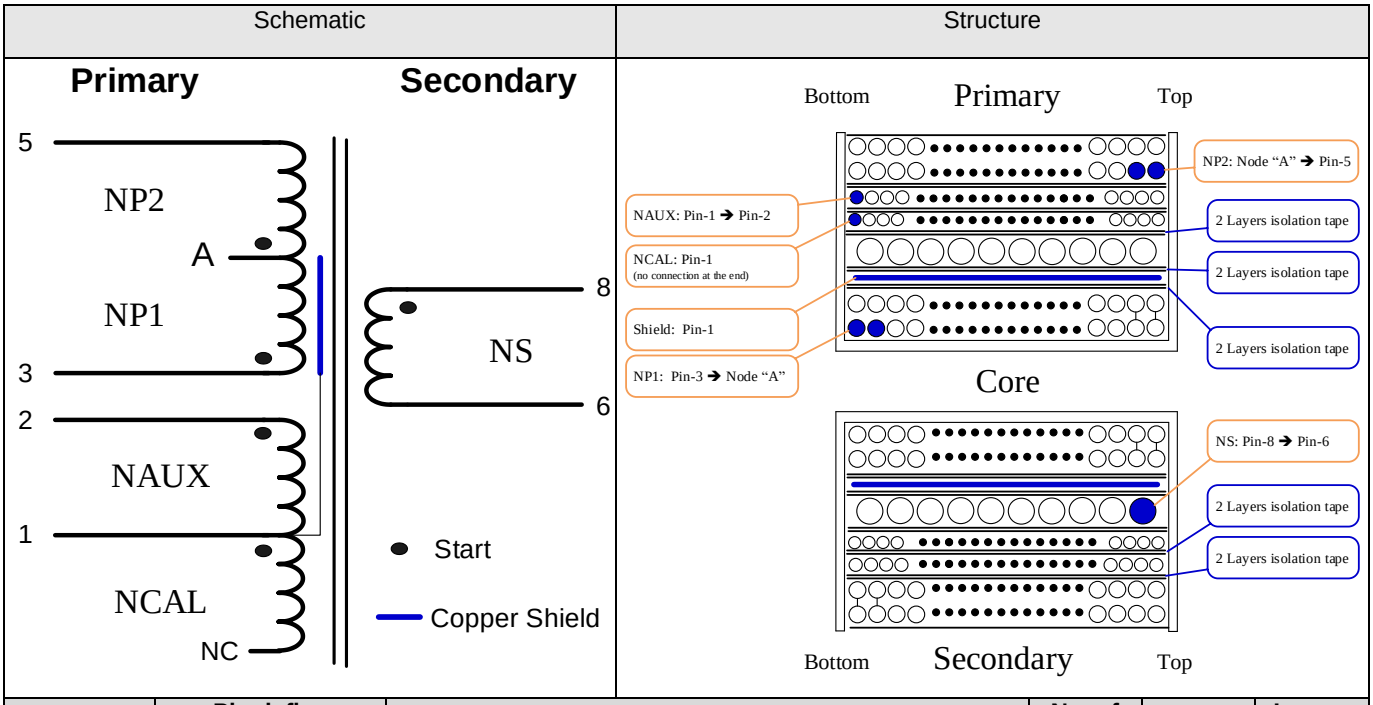
3.2 Bill of Material (BOM)

Item	Quantity	Reference	Description	Manufacturer Part Number	Manufacturer
1	**1**	**U1**	**AP3306, Active Clamping Flyback Controller**	**AP3306S10-13**	**Diodes Inc.**
2	**1**	**U2**	**APR340, SR Controller**	**APR340W6-7**	**Diodes Inc.**
3	**1**	**U3**	**AP43771V, Decoder IC**	**AP43771VFBZ-13**	**Diodes Inc.**
4	**1**	**Q2**	**High-Side Switch MOSFET, P-CH, 650V, SO-8, DMP65H9D0HSS-13**	**DMP65H9D0HSS-13**	**Diodes Inc.**
5	**1**	**Q4**	**MOSFET, N-CH, 30V, POWERDI3333-8, DMN3008SFG-13**	**DMN3008SFG-13**	**Diodes Inc.**
6	**3**	**D1,D2, D3**	**Fast Rectifier, 1A, 1000V, SOD-123, RS1MWF**	**RS1MWF-7**	**Diodes Inc.**
7	**1**	**D5**	**Switching Diode, SWD, 150mA, 75V, SOD123, 1N4148W**	**1N4148W-7-F**	**Diodes Inc.**
8	1	Q1	**Low-Side Switch GaN, 650V, PQFN 8X8, TP65H150LSG**	**TP65H150LSG**	**Transphorm***
9	1	Q3	MOSFET, N-CH, 100V, POWERDI5060-8, BSC035N10NS5	BSC035N10NS5	Infineon
10	**1**	**BD1**	**Bridge 3A 600V MSB30JL**	**MSB30JL**	**Diodes Inc.**
11	1	C1	EC 100uF 400V 12.5x42	SD400M101I40TA09S00R	Su'scon (冠坤)
12	3	C2A, C2B, C2C	MLCC 470nF 450V 1812 X7R C4532X7T2W474K230KE	C4532X7T2W474K230KE	TDK
13	1	C4	MLCC 10uF 35V 1206 X7R		
14	1	C5	MLCC 100pF 50V 0603 X7R		
15	1	C6	MLCC 4.7uF 35V 0805 X7R		
16	1	C8	MLCC 1nF 50V 0603 X7R		
17	1	C9	MLCC 2.2uF 100V 1206 X7R		
18	2	C10, C11	EC 330uF 25V 6.3x12 polymer		
19	4	C13, C13A, C13B, C13C	MLCC 10uF 25V 1206 X7R		
20	2	C14, C22	MLCC 4.7uF 10V 0805 X7R		
21	5	C15, C16, C19, C21, C24	MLCC 100nF 50V 0603 X7R		
22	1	C17	MLCC 2.2uF 50V 0805 X7R		
23	1	C18	MLCC 4.7nF 50V 0603 X7R		
24	1	C20	MLCC 1nF 250V 0805 X7R		
25	1	C23	MLCC 22nF 50V 0603 X7R		
26	1	CSN	MLCC 33nF 1KV 1210 X7R	C1210C333KDRACTU	KEMET
27	1	CX1	X2 0.33uF AC275V 13mm x 12.5mm x 6mm lead space 10mm		TENTA
28	1	CY1	Y1 1000pF AC300V	SMDDK1E3EA102M86RBH01	MuRata
29	1	F1	Fuse T3.15A 250V Time Lag	40013150000	Littlefuse
31	1	L1	Inductor 22uH	7447713220	Wurth Elektronik

32	1	NTC	NTC 100K 0603	NTCG103JF103FT1S	TDK
33	1	PC1	Optocoupler	TLV-1009	LITE ON
34	1	R2	RES 1K 0603 5%		
35	1	R3	RES 3R3 0805 5%		
36	3	R4, R7, R14	RES 100K 0603 1%		
37	1	R5	RES 20R 0805 1%		
38	1	R6	RES 2R2 0805 1%		
39	1	R8	RES 500mR 1206 1% 750mW	SMD12A1FR300T	Sart Tech
40	1	R9	RES 270mR 1206 1% 750mW	SMD12A1FR300T	Sart Tech
41	1	R12	RES 255K 0805 1%		
42	1	R13	RES 16K 0603 1%		
43	1	R15	RES 1K 0603 1%		
44	2	R16, R19	RES 10K 0603 1%		
45	1	R20	RES 10R 1206 5%		
46	1	RCS	RES 10mR 1206 1% Low CTR type		
47	1	T1	ATQ23/12.3 260uH		

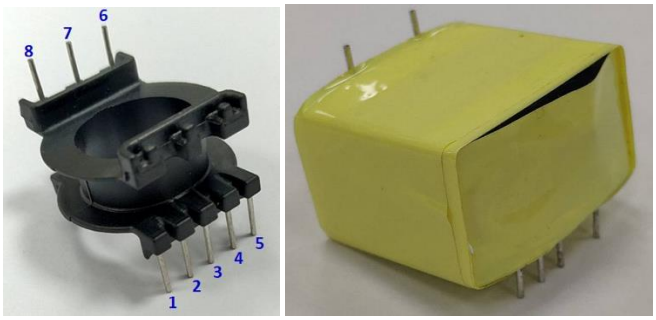
SuperGaN® Power FETs is the trademark of Transphorm Inc. Detailed product information can be found on https://www.transphormusa.com//

3.3 Transformer Design



Definition	Pin define (Start >> End)	Wire (φ)	No. of Turns	Layers	Layers of Tape
NP1	3 → Node A	2UEW Litz Wire, 0.1mmx18, 1P, Bot -> Top -> Bot	14	2	1 L
Shield	1 → NC	5mm width copper shielding, solder to pin-1.	1	1	1 L
NS	8 → 6	TRW(B), Triple Insulated Litz Wire 0.25x7, 1P	5	1	1 L
NCAL	1 → NC	2UEW, 0.13, 1P	20	1	1 L
NAUX	2 → 1	2UEW, 0.13, 2P	12	1	1 L
NP2	Node A → 5	2UEW Litz Wire, 0.1mmx18, 1P, Bot -> Top -> Bot	14	2	2L

BOBBIN PIN Define:



Item	Test Condition	Rating
Primary Inductance	Pin 3-5,all other windings open, measured at 100kHz / 1V	260μH+/- 5%
Note	Bobbin: 裕龍鑫科技, ATQ2327 Core： A-Core(安磁), ATQ-23/12.3 (JPP-96F)	

3.4 Schematics Description

3.4.1 AC Input Circuit & Differential Filter

The Fuse F1 protects against overcurrent conditions which occur when some main components fails. The NF1 and NF2 are common mode chocks for the common mode noise suppression. The BD is a bridge rectifier which converts alternating current and voltage into direct current and voltage. The CE1~CE4, L1, CE5~CE6 are composed of the Pi filter for filtering the differential switching noise back to AC source.

3.4.2 AP3306 PWM Controller

AP3306, a highly integrated Active Clamp Flyback (ACF) controller, integrates high-voltage start-up function through HV pin and X-Cap discharging function. It also integrates a VCCL LDO circuit, which allows the LDO to regulate the wide range VCCL to an acceptable value. This makes AP3306 an ideal candidate for wide range output voltage applications such as USB-PD3.0 PPS. With embedded high-side and low-side switch control mechanism, AP3306 provides proper timing sequences to control Q3 (high-side Switch) and Q4 (low-side Switch) operations to implement two key efficiency improvement approaches, namely, ZVS (Zero Voltage Switching) and leakage energy recycling (stored in Csn) to achieve high-power density charger applications. At no load or light load, the AP3306 will enter the burst mode to minimize standby power consumption.

3.4.3 APR340 Synchronous Rectification (SR) MOSFET Driver

As a high-performance solution, APR340 is a secondary side SR controller to effectively reduce the secondary side rectifier power dissipation which works in DCM operation.

3.4.4 AP43771V PD 3.0 Decoder & Protection on/off N MOSFET and Interface to Power Devices

Few important pins provide critical protocol decoding and regulation functions in AP43771V:

1) **CC1 & CC2 (Pin 11, 10)**: CC1 & CC2 (Configuration Channel 1 & 2) are defined by USB Type-C spec to provide the channel communication link between power source and sink device.
2) **Constant Voltage (CV)**: The CV is implemented by sensing VFB (pin 8) and comparing with internal reference voltage to generate a CV compensation signal on the OCDRV pin (pin 5). The output voltage is controlled by firmware through CC1/CC2 channel communication with the sink device.
3) **Constant Current (CC)**: The CC is implemented by sensing the current sense resistor (RCS, 10mΩ, 1%, Low TCR) and compared with internal programmable reference voltage. The output current is controlled by firmware through CC1/CC2 channel communication with the sink device.
4) **Loop Compensation:**
   R19 & C19 form the voltage loop compensation circuit, and C18 form the current loop compensation circuit.
5) **OCDRV (Pin5)**: It is the key interface link from secondary decoder (AP43771V) to primary regulation circuit (AP3306). It is connected to Opto-coupler PC1 Pin 2 (Cathode) for feedback information based on all sensed CC1 & CC2 signals for getting desired Vbus voltage & current.
6) **PWR_EN (Pin2) to N-MOSFET Gate**: The pin is used to turn on/off N-MOSFET (Q1) to enable/disable voltage output to the Vbus.

Chapter 4 The Evaluation Board (EVB) Connections

4.1 EVB PCB Layout

Main Board – 1

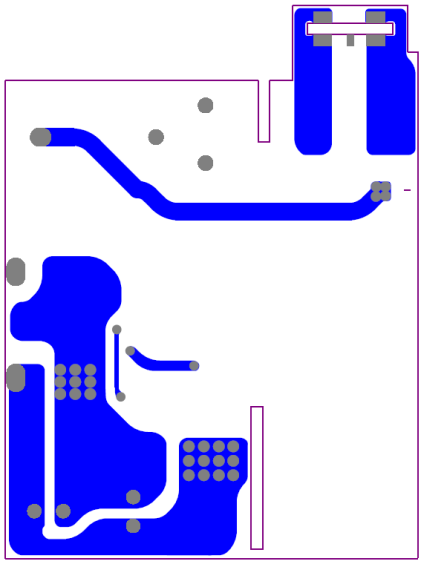


Figure 4: PCB Layout Top View

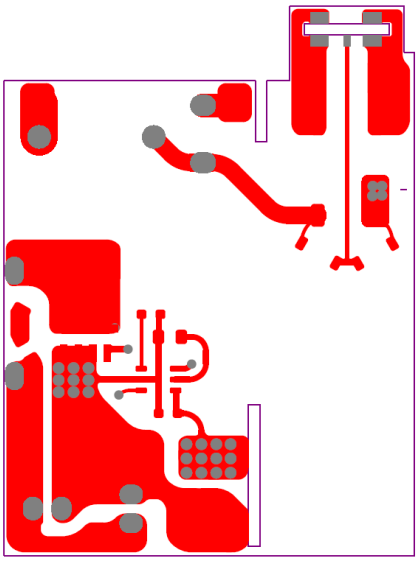


Figure 5: PCB Layout Bottom View

Main Board – 2

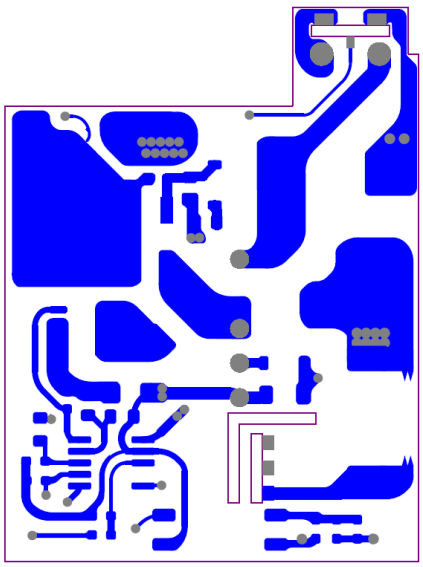


Figure 6: PCB Layout Top View

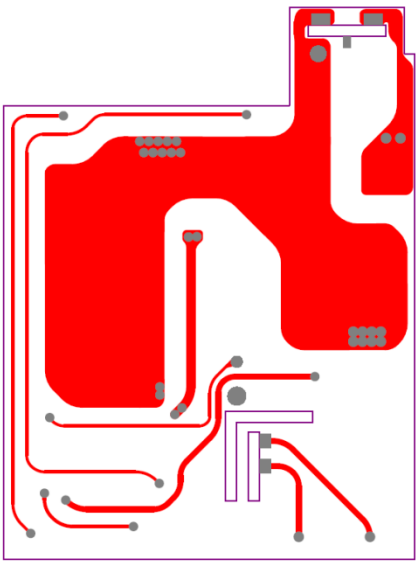


Figure 7: PCB Layout Bottom View

Main Board – 3

Figure 8: PCB Layout Top View

Figure 9: PCB Layout Bottom View

Daughter Board

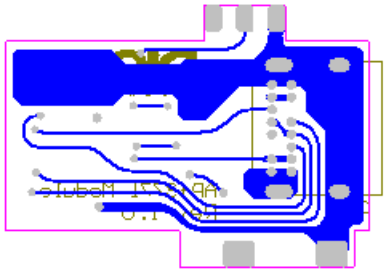


Figure 10: PCB Layout Top View

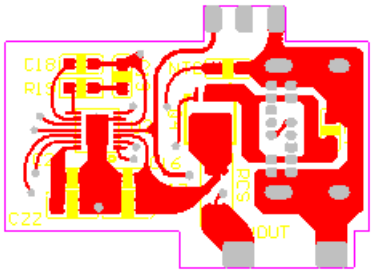


Figure 11: PCB Layout Bottom View

4.2 Quick Start Guide before Connection

1) Before starting the 65W EVB test, the end user needs to prepare the following tools, software and manuals.

For details, please consult USBCEE sales through below link for further information.

USBCEE PD3.0 Test Kit: USBCEE Power Adapter Tester. https://www.usbcee.com/product-details/4

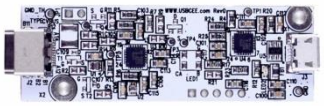
USBCEE PAT Tester	GUI Display	USB-A to Micro-B Cable	Type-C Cable
			

Figure 12: Test Kit / Test Cables

2) Prepare a certified three-foot Type-C cable and a Standard-A to Micro-B Cable.

3) Connect the AC inputs: L & N wires of EVB to AC power supply output “L and N “wires.

4) Ensure that the AC source is switched OFF or disconnected before the connection steps.

5) A type-C cable for the connection between EVB’s and Type-C receptacles of test kit.

6) Output of Type-C port & USB A-port are connected to E-load + & - terminals by cables.

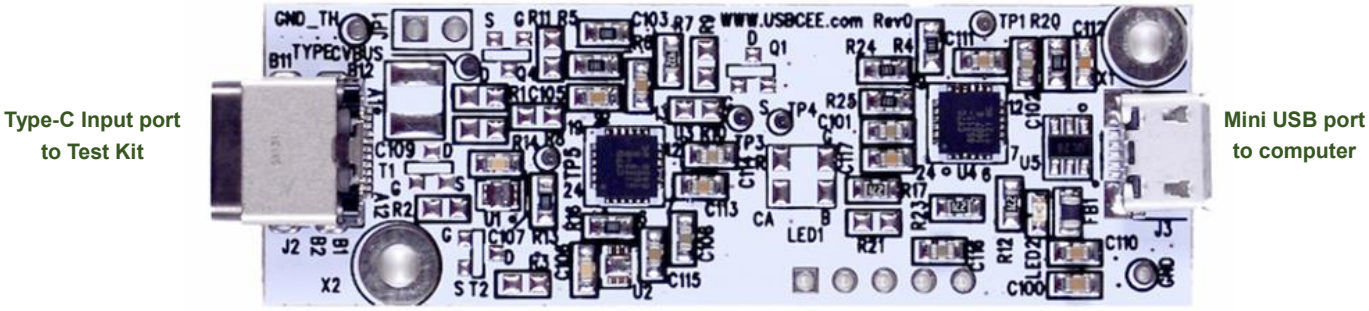


Figure 13: The Test Kit Input & Output and E-load Connections

4.3 Connection with E-Load

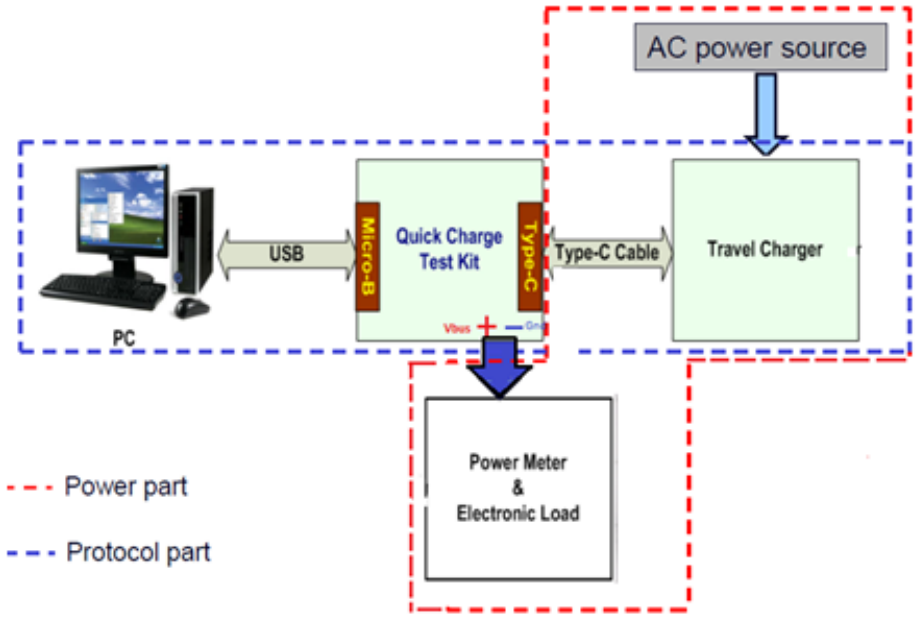


Figure 14: Diagram of Connections in the Sample Board

Chapter 5 Testing the Evaluation Board

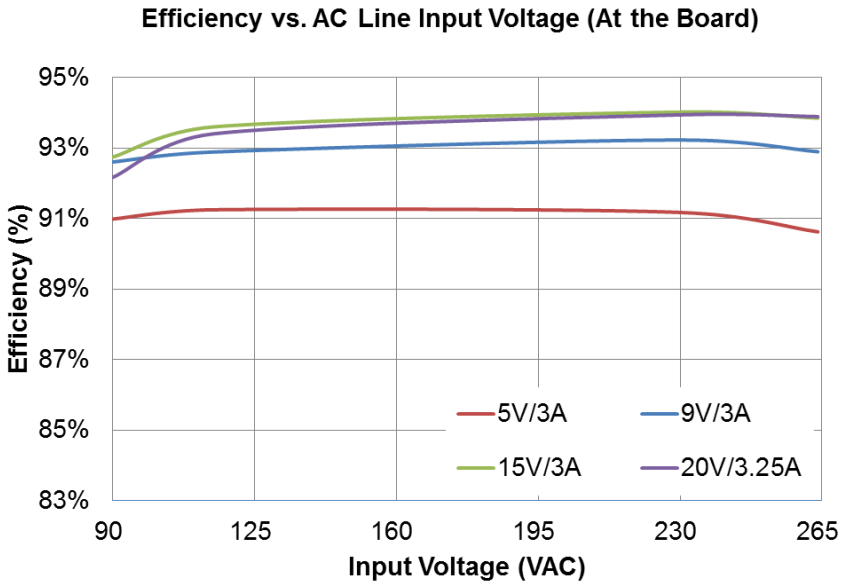
5.1 Input & Output Characteristics

5.1.1 Input Standby Power

Vin(Vac)	F(Hz)	Pin(mW)
90	**63**	13.37
115	**60**	13.95
230	**50**	18.30
264	**47**	21.31

5.1.2 Multiple Output Full Load Efficiency at Different AC Line Input Voltage

Vin(Vac)	F(Hz)	Iout(A)	Vout_Board (V)	Pin(W)	Pout(W)	Eff(%)
90	60	3.25	20.032	70.64	65.10	92.16%
115	60	3.25	20.080	69.87	65.26	93.40%
230	50	3.25	20.091	69.51	65.30	93.94%
264	50	3.25	20.089	69.54	65.29	93.89%
90	60	3.00	15.142	48.98	45.41	92.74%
115	60	3.00	15.152	48.57	45.42	93.60%
230	50	3.00	15.159	48.37	45.44	94.02%
264	50	3.00	15.156	48.45	45.43	93.85%
90	60	3.00	9.236	29.92	27.70	92.60%
115	60	3.00	9.240	29.84	27.71	92.89%
230	50	3.00	9.239	29.73	27.71	93.23%
264	50	3.00	9.236	29.83	27.70	92.89%
90	60	3.00	5.280	17.41	15.84	90.99%
115	60	3.00	5.280	17.36	15.84	91.25%
230	50	3.00	5.281	17.38	15.84	91.17%
264	50	3.00	5.280	17.48	15.82	90.62%



5.1.3 Multiple Output Average Efficiency at Different Loading

Port-C PD3.0_PDO_20V / 15V Average Efficiency

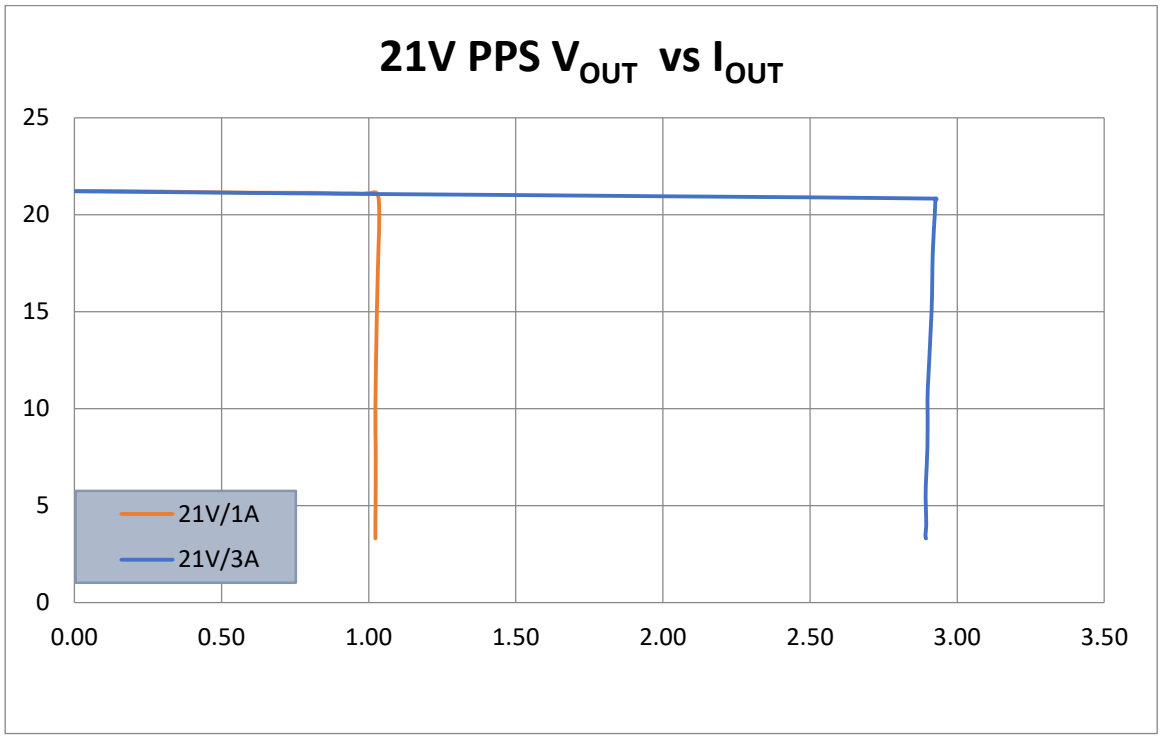
PDO Mode	Vin (Vac)	F(Hz)	Remarks	Iout(A)	Vout(V)	Pin(W)	Pout(W)	Eff(%)	Average Efficiency
20V/3.25A	115	60	100%	3.250	20.080	69.87	65.26	93.40%	93.55%
			75%	2.435	20.047	52.04	48.81	93.80%	
			50%	1.625	19.987	34.66	32.48	93.72%	
			25%	0.810	19.929	17.30	16.14	93.29%	
			10%	0.325	19.895	7.10	6.47	91.06%	
	230	50	100%	3.250	20.091	69.51	65.30	93.94%	93.41%
			75%	2.435	20.038	51.97	48.79	93.88%	
			50%	1.625	19.985	34.78	32.48	93.37%	
			25%	0.810	19.921	17.45	16.14	92.46%	
			10%	0.325	19.888	7.23	6.46	89.43%	
15V/3A	115	60	100%	3.000	15.152	48.57	45.46	93.60%	93.51%
			75%	2.250	15.097	36.27	33.97	93.64%	
			50%	1.500	15.036	24.09	22.55	93.62%	
			25%	0.750	14.973	12.05	11.23	93.17%	
			10%	0.300	14.941	4.94	4.48	90.79%	
	230	50	100%	3.000	15.159	48.37	45.48	94.02%	93.68%
			75%	2.250	15.097	36.17	33.97	93.93%	
			50%	1.500	15.032	24.05	22.55	93.75%	
			25%	0.750	14.975	12.07	11.23	93.02%	
			10%	0.300	14.940	5.00	4.48	89.67%	

Port-C PD3.0_PDO_9V / 5V Average Efficiency

PDO Mode	Vin (Vac)	F(Hz)	Remarks	Iout(A)	Vout(V)	Pin(W)	Pout(W)	Eff(%)	Average Efficiency
9V/3A	115	60	100%	3.000	9.240	29.84	27.72	92.89%	92.92%
			75%	2.250	9.176	22.18	20.65	93.07%	
			50%	1.500	9.112	14.68	13.67	93.10%	
			25%	0.750	9.047	7.32	6.79	92.64%	
			10%	0.300	9.008	3.06	2.70	88.22%	
	230	50	100%	3.000	9.239	29.73	27.72	93.23%	92.92%
			75%	2.250	9.174	22.15	20.64	93.18%	
			50%	1.500	9.111	14.68	13.67	93.11%	
			25%	0.750	9.047	7.36	6.79	92.18%	
			10%	0.300	9.007	3.02	2.70	89.46%	
5V/3A	115	60	100%	3.000	5.280	17.36	15.84	91.25%	91.08%
			75%	2.250	5.217	12.85	11.74	91.37%	
			50%	1.500	5.155	8.46	7.73	91.42%	
			25%	0.750	5.091	4.23	3.82	90.27%	
			10%	0.300	5.050	1.72	1.52	88.24%	
	230	50	100%	3.000	5.281	17.38	15.84	91.17%	90.68%
			75%	2.250	5.217	12.87	11.74	91.19%	
			50%	1.500	5.155	8.50	7.73	90.99%	
			25%	0.750	5.091	4.27	3.82	89.37%	
			10%	0.300	5.049	1.72	1.51	87.95%	

5.1.4 PD3.0 & PPS Compatible Mode Testing

CC Mode current limitation function testing
The test is by USBCEE Tester and with E-Load set at CR mode.
To Port-C PPS Mode set 21V-1A & 21V-3A and then increase the current (by reducing R) to see the CC-CV curve



5.2 Key Performance Waveforms

5.2.1 65W PD3.0 System Start-up Time

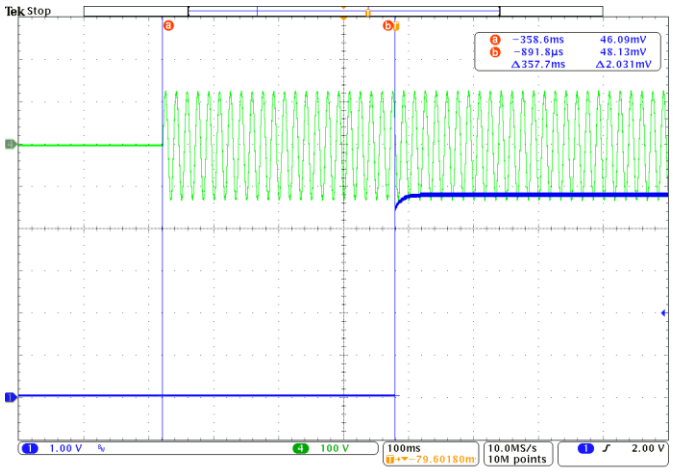


Figure 15: Turn on time is 357.7ms at Full Load@ 90Vac

5.2.2 Q1 / Q2 / Q3 MOSFET Voltage Stress at Full Load @264Vac

Primary side MOSFET : Q1 & Q2 and Secondary side SR MOSFET- Q3

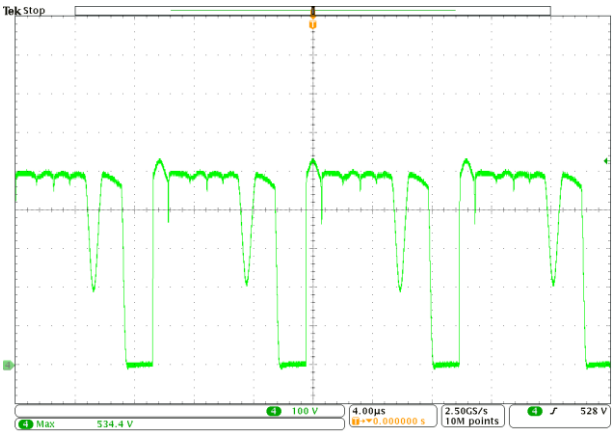


Figure 16: Q1 Vds Voltage stress

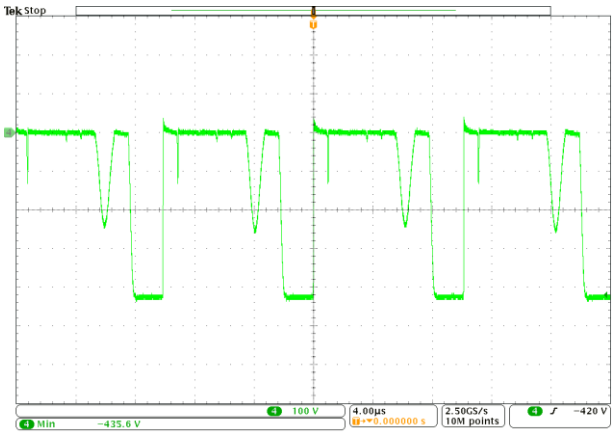


Figure 17: Q2 Vds Voltage stress

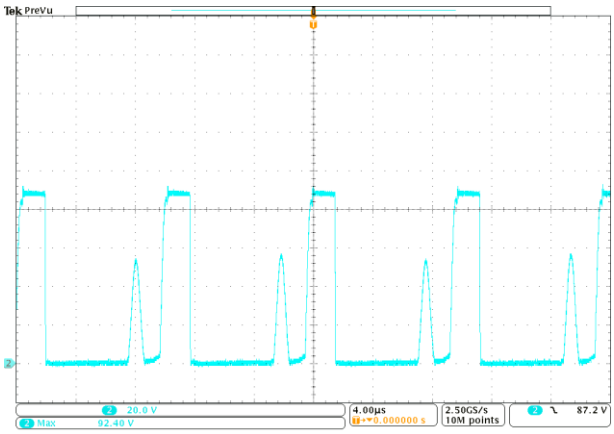


Figure 18: Q3 Vds Voltage stress

Component	Vout	Vds	Vds_Max_Spec	Ratio of voltage stress
Q1	20V	534V	650V	82.21%
Q2		-436V	- 650V	66.92%
Q3		92.4V	100V	92.40%

5.2.3 System Output Ripple & Noise with the Cable

Connect 47μF AL Cap and 104MLCC to the cable output unit in parallel

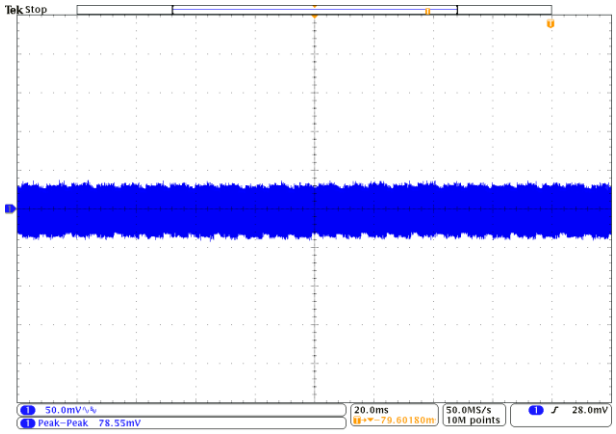


Figure 19: 90Vac/60Hz@ 5V/3A ΔV=78.55mV

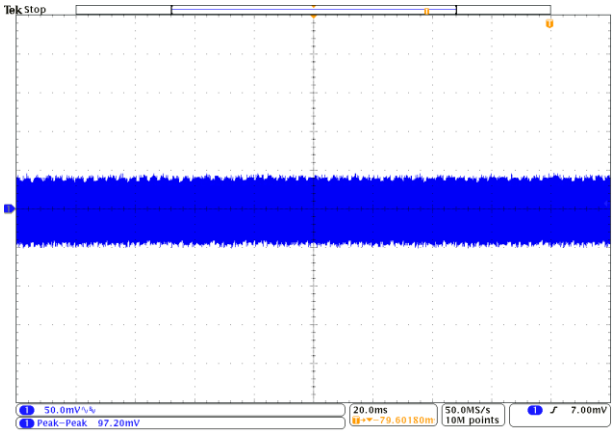


Figure 20: 264Vac/50Hz@5V/3A ΔV=97.20mV

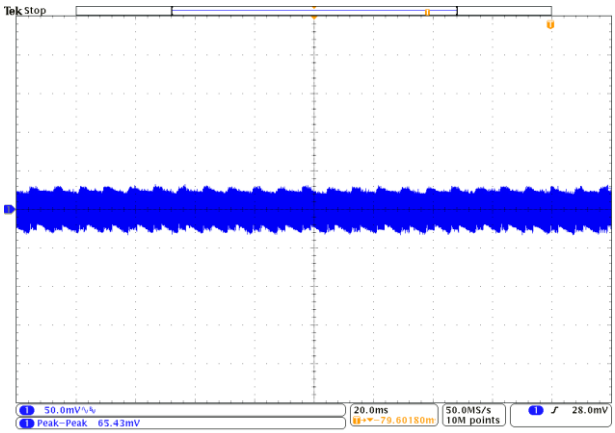


Figure 21: 90Vac/60Hz@9V/3A ΔV=65.43mV

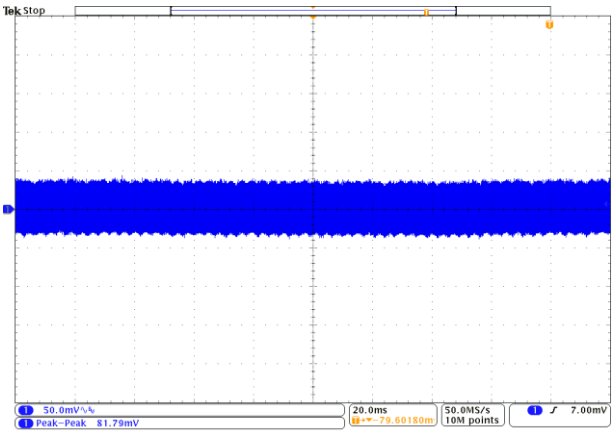


Figure 22: 264Vac/50Hz@9V/3A ΔV=81.79mV

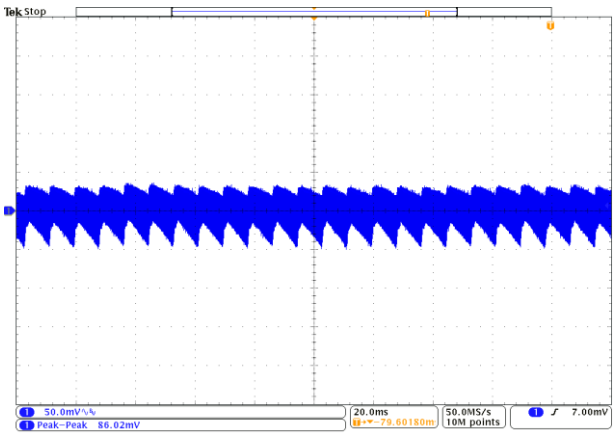


Figure 23: 90Vac/60Hz@15V/3A ΔV=86.02mV

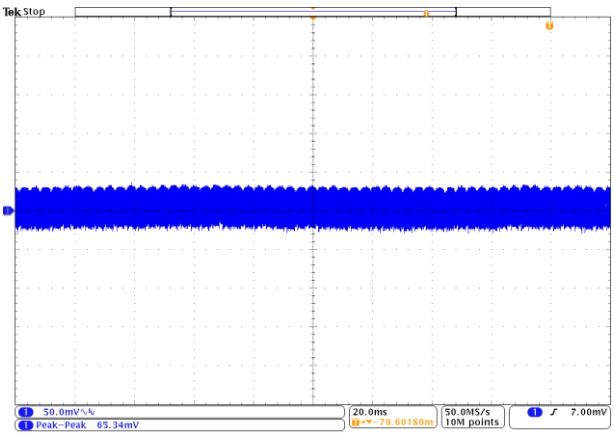


Figure 24: 264Vac/50Hz@15V/3A ΔV=65.34mV

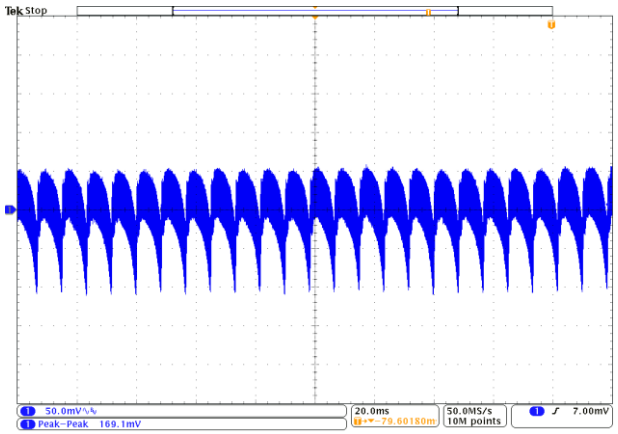


Figure 25: 90Vac/60Hz@20V/3.25A ΔV=169.1mV

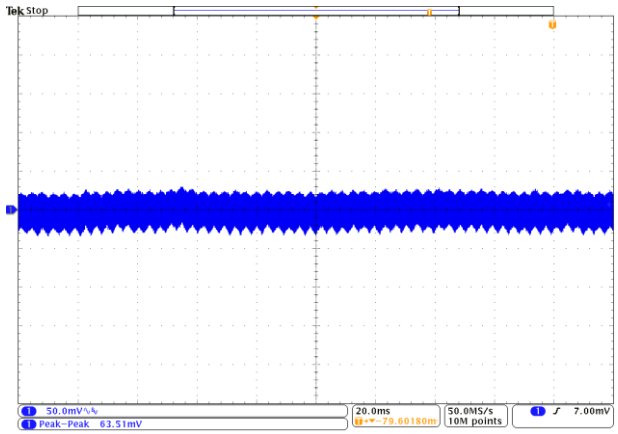


Figure 26: 264Vac/50Hz@20V/3.25A ΔV=63.51mV

5.2.4 Dynamic load ----0% Load~100% Load, T=20mS, Rate=15mA/μS (PCB End)

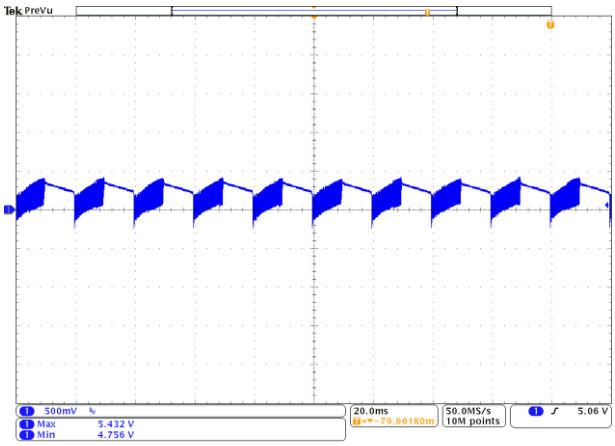


Figure 27: 90Vac/60Hz Port-C@ Vout=5V

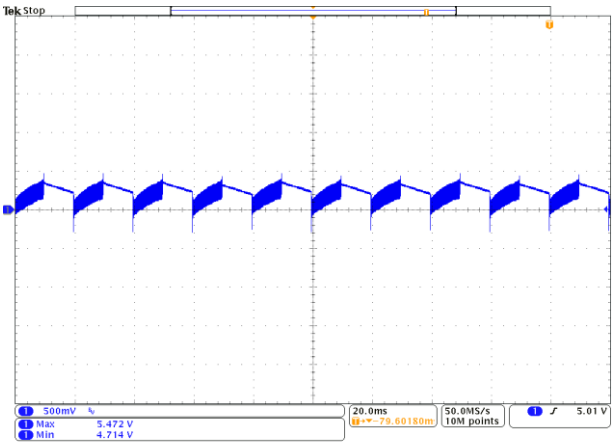


Figure 28: 264Vac/50Hz Port-C@ Vout=5V

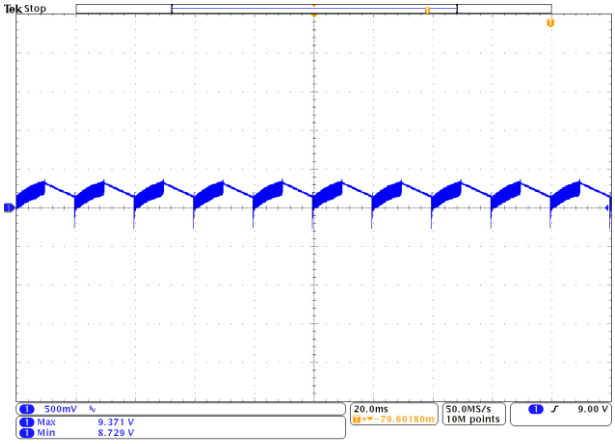


Figure 29: 90Vac/60Hz Port-C@ Vout=9V

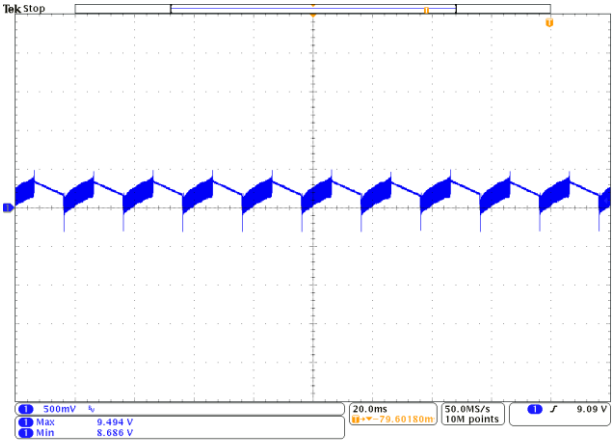


Figure 30: 264Vac/50Hz Port-C@ Vout=9V

	Vo_ Undershoot(V)	Vo_ Overshoot(V)		Vo_Undershoot(V)	Vo_Overshoot(V)
Vin=90Vac@5V	4.756	5.432	Vin=90Vac@9V	8.729	9.371
Vin=264Vac@5V	4.714	5.472	Vin=264Vac@9V	8.686	9.494

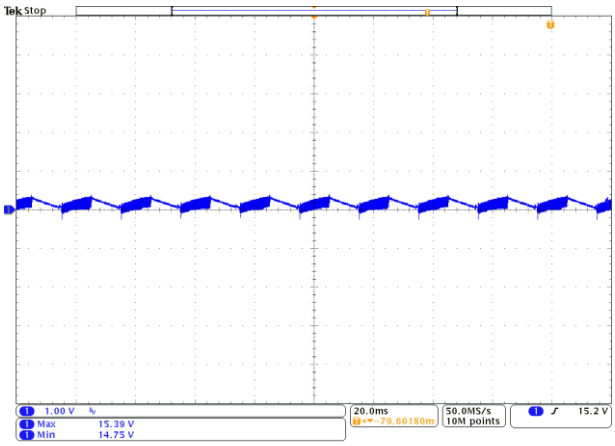


Figure 31: 90Vac/60Hz Port-C@ Vout=15V

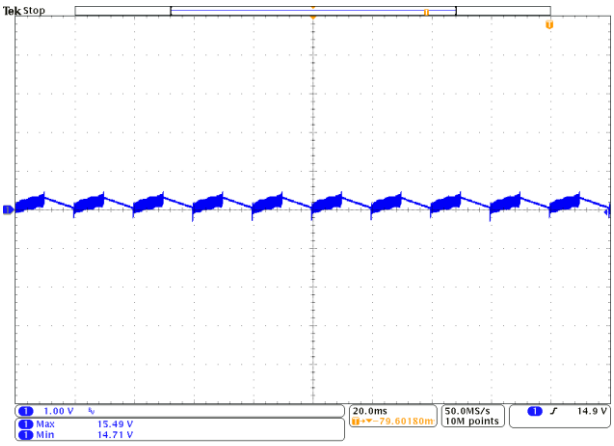


Figure 32: 264Vac/50Hz Port-C@ Vout=15V

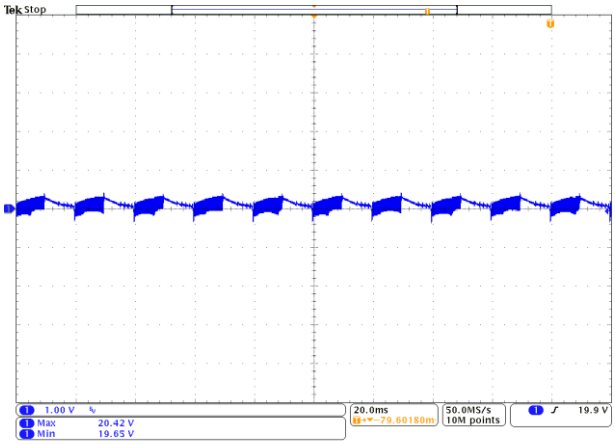


Figure 33: 90Vac/60Hz Port-C@ Vout=20V

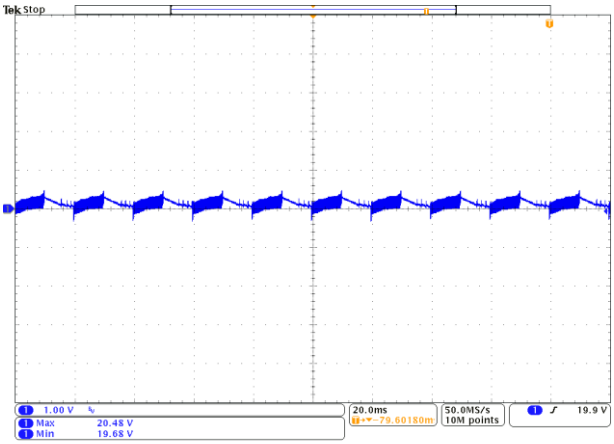


Figure 34: 264Vac/50Hz Port-C@ Vout=20V

	Vo_ Undershoot(V)	**Vo_ Overshoot(V)**		**Vo_Undershoot(V)**	**Vo_Overshoot(V)**
Vin=90Vac@15V	14.75	15.39	Vin=90Vac@20V	14.71	15.49
Vin=264Vac@15V	19.65	20.42	Vin=264Vac@20V	19.68	20.48

5.2.5 Output Voltage Transition Time from Low to High

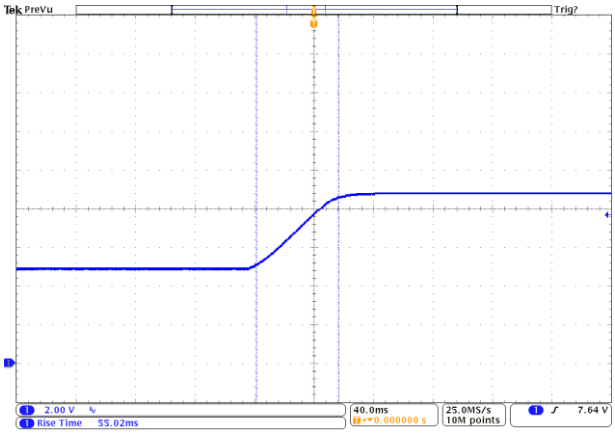


Figure 35: 5V→9V Rise Time = 55.02ms @90Vac

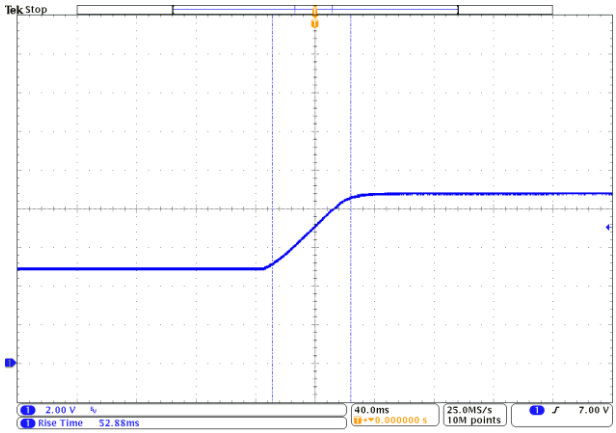


Figure 36: 5V→9V Rise Time = 52.88ms @264Vac

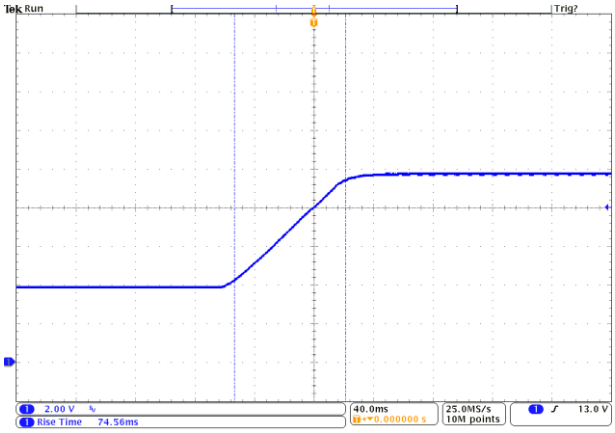


Figure 37: 9V→15V Rise Time = 74.56ms @90Vac

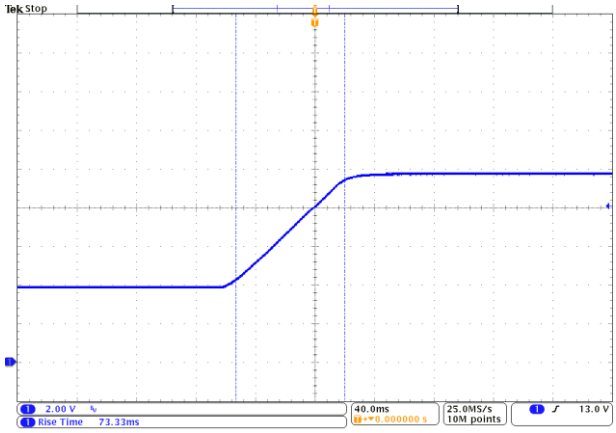


Figure 38: 9V→15V Rise Time = 73.33ms @264Vac

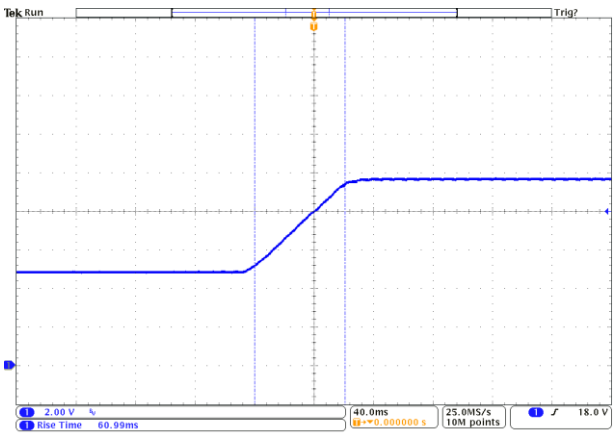


Figure 39: 15V→20V Rise Time = 60.99ms @90Vac

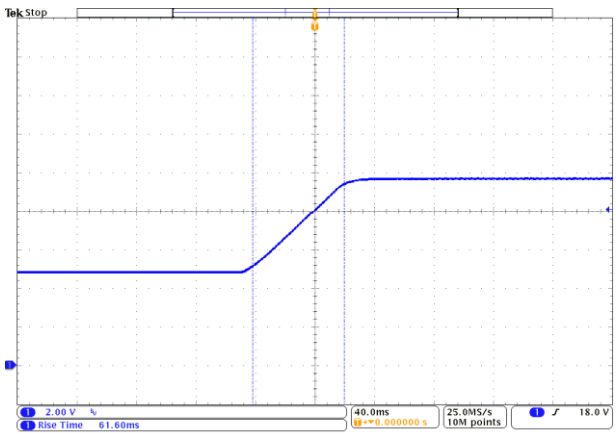


Figure 40: 15V→20V Rise Time = 61.60 ms @264Vac

5.2.6 Output Voltage Transition Time from High to Low

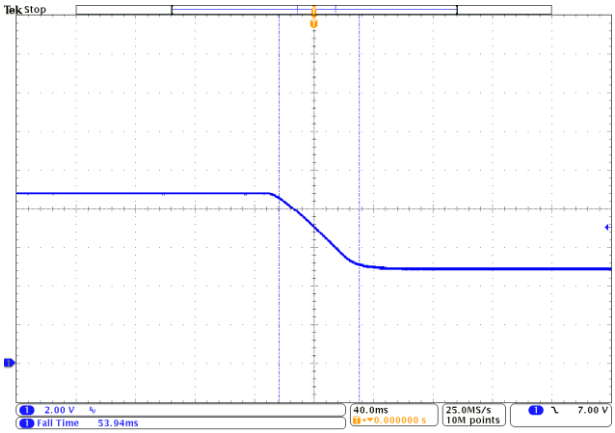


Figure 41: 9V→5V Fall Time = 53.94ms @90Vac

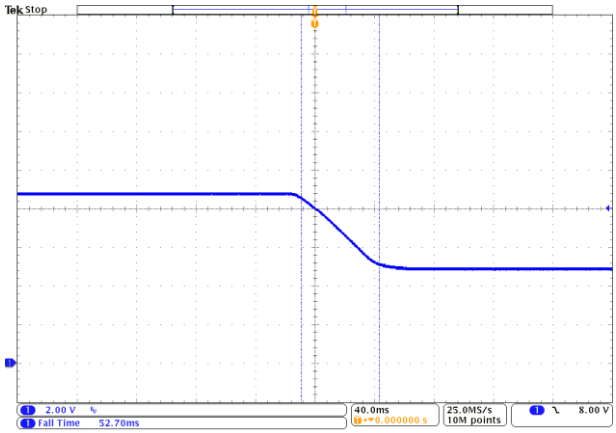


Figure 42: 9V→5V Fall Time = 5 2.70ms @264Vac

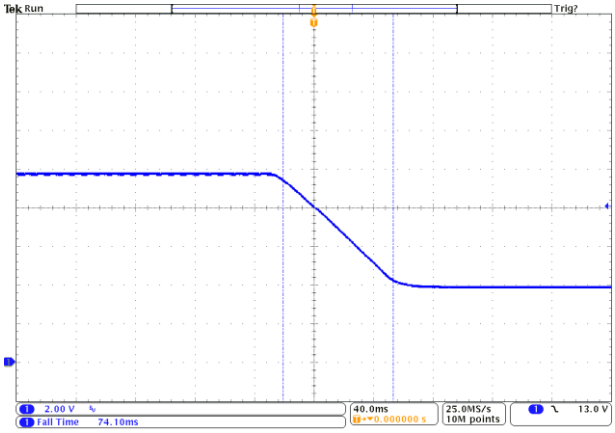


Figure 43: 15V→9V Fall Time = 74.10ms @90Vac

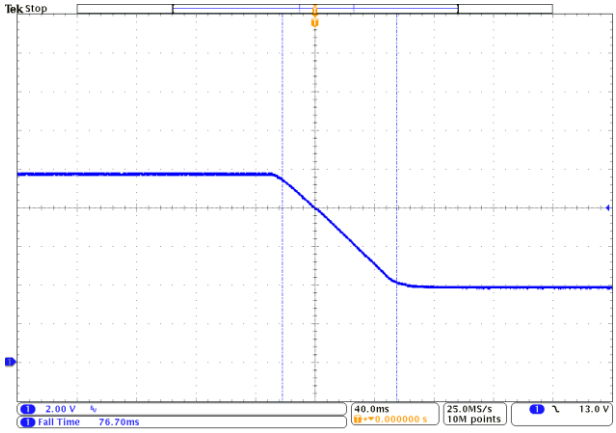


Figure 44: 15V→9V Fall Time = 76.70ms @264Vac

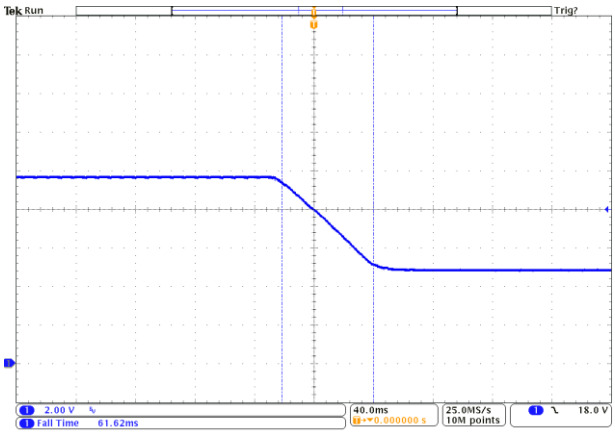


Figure 45: 20V→15V Fall Time = 61.62ms @90Vac

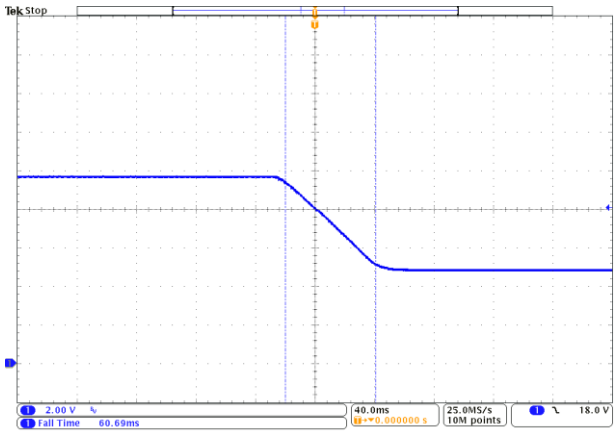


Figure 46: 20V→15V Fall Time = 60.69ms @264Vac

5.2.7 Thermal Testing

Output Condition : 20V/3.25A

Main Voltage	Temperature (°C)					
	BD1	Q1	Q2	Q3	U1	U2
90Vac/60Hz	108.6	94.0	104.7	92.1	94.2	88.7

Test Condition: Vin=90Vac @ 20V-3.25A Full load Open Frame

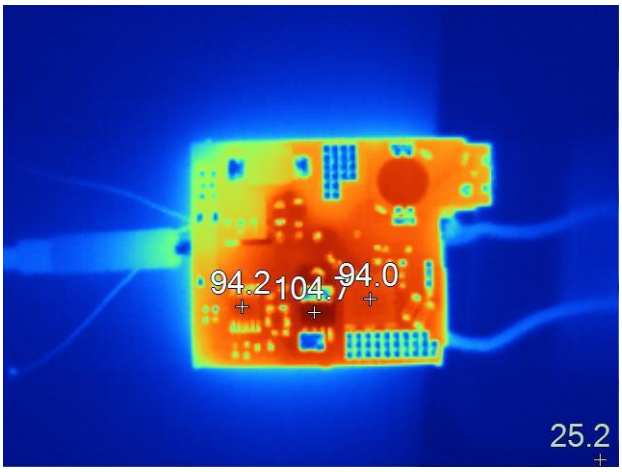


Figure 47: Top Components side

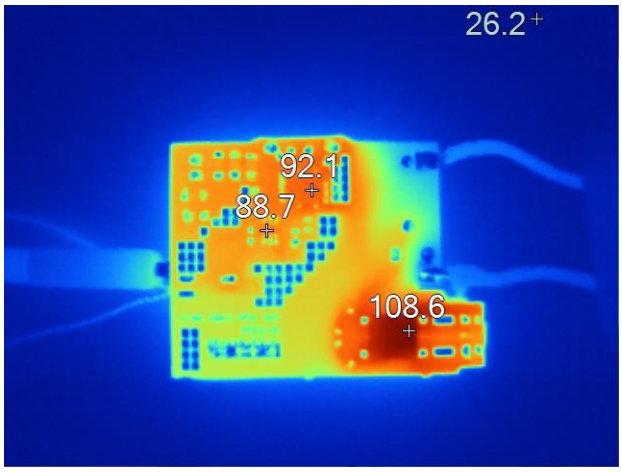


Figure 48: Bottom Suface Mount side

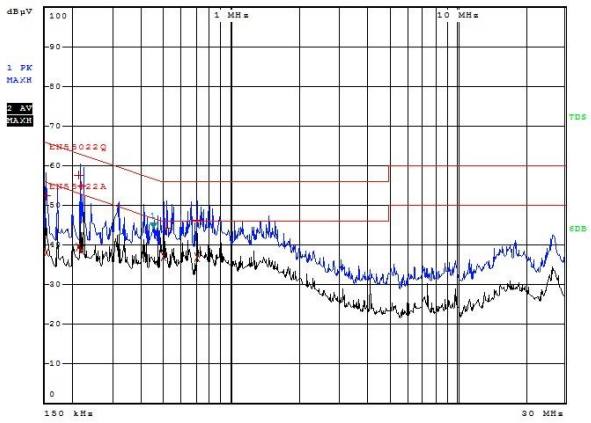
BD1: Bridge Rectifier
Q1 : Primary Side High Voltage GaN FET
Q2 : Primary Side High Voltage P-MOS
Q3 : Secondary Side Sync-Rectifier
U1 : AP3306, ACF Controller
U2 : APR340, Sync-Rectifier Controller

Note: Component temperature can be further optimized with various system design and thermal management approaches by manufacturers.

5.3 EMI (Conduction) Testing

5.3.1 115Vac testing results

Output Condition : 20V/3.25A

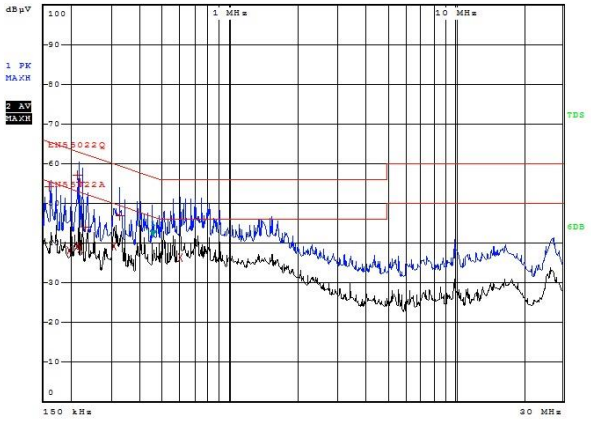


EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	154 kHz	52.26	-13.51
2	Average	154 kHz	38.16	-17.61
1	Quasi Peak	214 kHz	57.65	-5.39
2	Average	214 kHz	39.37	-13.67
1	Quasi Peak	222 kHz	54.95	-7.79
2	Average	222 kHz	38.75	-13.99
2	Average	502 kHz	37.17	-8.82
1	Quasi Peak	518 kHz	44.25	-11.74
1	Quasi Peak	706 kHz	46.27	-9.72
2	Average	706 kHz	36.79	-9.20

Figure 49: 115Vac/60Hz L line



EDIT PEAK LIST (Final Measurement Results)

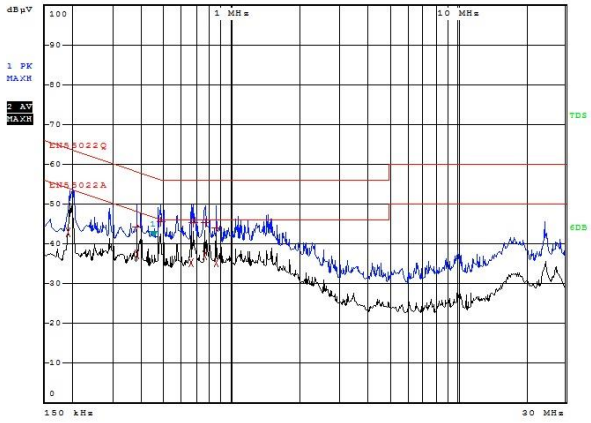
Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	162 kHz	54.09	-11.26
2	Average	198 kHz	38.18	-15.51
1	Quasi Peak	214 kHz	56.97	-6.07
2	Average	214 kHz	39.22	-13.52
1	Quasi Peak	222 kHz	55.27	-7.47
2	Average	222 kHz	38.75	-13.98
1	Quasi Peak	234 kHz	43.87	-18.43
2	Average	310 kHz	39.12	-10.54
1	Quasi Peak	326 kHz	46.90	-12.65
2	Average	606 kHz	36.40	-9.59

Figure 50: 115Vac/60Hz N line

5.3.2 230Vac testing results

Output Condition : 20V/3.25A

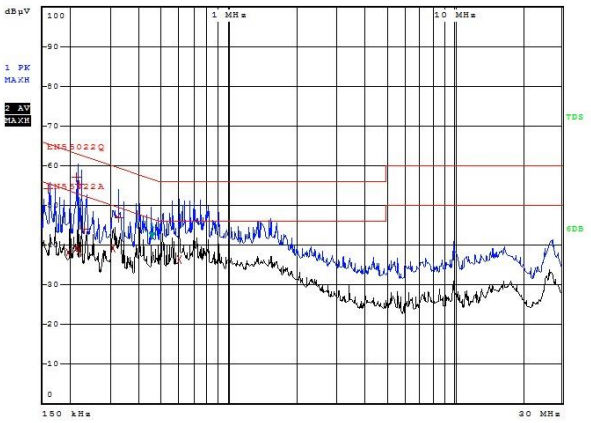


EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	194 kHz	43.01	-10.85
1	Quasi Peak	382 kHz	44.30	-13.93
2	Average	382 kHz	37.30	-10.93
1	Quasi Peak	486 kHz	45.51	-10.71
2	Average	662 kHz	35.39	-10.60
1	Quasi Peak	678 kHz	45.30	-10.69
2	Average	766 kHz	37.11	-8.88
1	Quasi Peak	774 kHz	45.19	-10.80
1	Quasi Peak	858 kHz	43.95	-12.04
2	Average	858 kHz	35.29	-10.70

Figure 49: 230Vac/50Hz L line



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	198 kHz	52.34	-11.35
2	Average	198 kHz	44.02	-9.66
2	Average	286 kHz	39.36	-11.27
1	Quasi Peak	474 kHz	44.74	-11.70
2	Average	474 kHz	36.64	-9.80
1	Quasi Peak	690 kHz	46.08	-9.91
2	Average	690 kHz	36.93	-9.07
1	Quasi Peak	786 kHz	45.49	-10.50
1	Quasi Peak	866 kHz	42.80	-13.19
2	Average	1.302 MHz	33.10	-12.89

Figure 50: 230Vac/50Hz N line

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