Solutions to Current High-Speed Board Design

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Introduction

Today's board design is not as simple as it was in the past. Current high-speed designs demand a board designer's extensive knowledge of these issues: transmission line effect, EMI, and crosstalk. The designer also needs to be an expert concerning board material, signal and power stacking, connectors, cables, vias, and trace dimensions.

Pericom offers an extensive line of clock products for desktop, notebook, set-top boxes, information devices, servers, and workstations. This application note will help a designer ensure proper termination, placement, routing, and stacking of the board to ensure proper data transfers between the microprocessor, cache, main memory, and expansion busses.

Q. Is this a transmission line or a two wire interconnect?

This is a very important question that we need to answer before starting a PCB design. It is crucial because transmission lines act differently than a simple wire.

If we have a 100 Hz circuit that is driving a 1 Meg Ohm load through a one meter wire, then the resistivity of the line is negligible compared to the load. The equation $V = V_0(1\text{-}e^{-\frac{t}{RC}})$ is used to determine the characteristic of the signal. The step voltage input will be delayed by the RC constant.

If, however, this circuit is running at 100 MHz, then the analysis shown above does not work and we need to treat this as a transmission line. We have to use Transmission Line Theory to determine the response of this circuit. If this transmission line is not terminated properly, you will have the following to contend with: ringing delays, overshoot, and undershoot. Other conditions that could affect your circuit are crosstalk, driver overload, and reduced noise margins. Any of which will ensure that your board is not working properly.

Q. How do we determine if this is a transmission line?

The length of the interconnection and the frequency of the circuit is the answer. If the length of the interconnection is larger than a tenth of the signal's sinusoidal wavelength, you will have to rely on transmission line theory. For example, if you have a 32-inch long interconnect when the frequency is higher then 25 MHz, you can treat the interconnect as a transmission line. If it is 24 MHz and lower, it is a lumped circuit.

The analysis below will explain it further:

$\lambda = CT$ or $\lambda = C/F$

$\lambda = 320$ inches $= 8.2$ m

$C = C_0\sqrt{(\varepsilon_R)}$, for cable $\varepsilon_R = 2.3$

$F = C/\lambda = 300x10^6 / 8.2\sqrt{2.3} = 24$ MHz

Following are the wavelengths for various frequencies:

$\lambda = 300 \times 10^6/100$ Hz $= 3000$ Km

$\lambda = 300 \times 10^6/100$ MHz $= 3$m

$\lambda = 300 \times 10^6/1$ GHz $= 30$cm

If you have a signal that is 10 GHz, 1 GHz, and 100 MHz, the waveforms are shown in Figure 1 through a 2-cm-long resistor. Notice that at 1 GHz the current differs slightly at each end. At 10 GHz you cannot define the current at one end or the other.

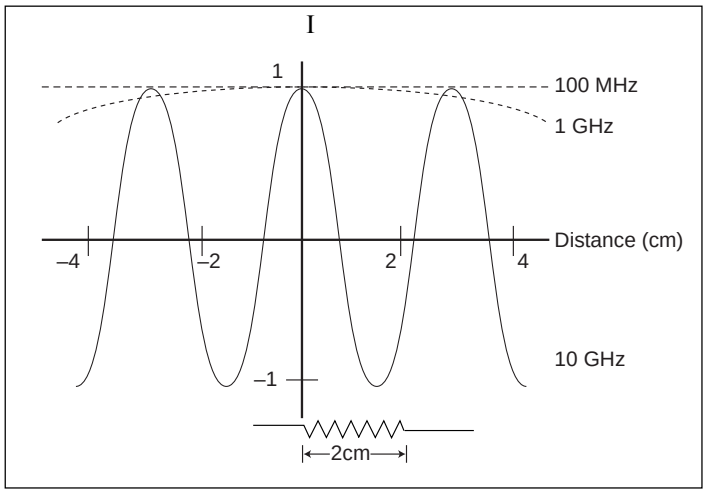

Figure 1.

When discussing digital design, to determine the interconnection type, using the signal's rise time is easier then relying on the wavelength.

Transmission line theory should be used when the signal's rise time is less then twice the propagation time Tp, or time of flight for the signal's electromagnetic wave to reach the end of the interconnect.

Consider the 32-inch and the 24 MHz in the previous example

Tp = distance/velocity

Tp= 81 cm x/$\sqrt{(2.3)}$ /300x10^6 = 4.15ns

This is the time it takes the magnetic wave to make a one-way trip.

2Tp = 8.3ns time it takes to make 2-way trip.

If the rise time is less then 8.3ns, it is a transmission line. If the rise is 20 percent of the period, then tr = 0.2 x 8.3ns. Then T = 41.5ns and F=24MHz.

To save time in determining when to use transmission line theory, refer to the figure shown below.

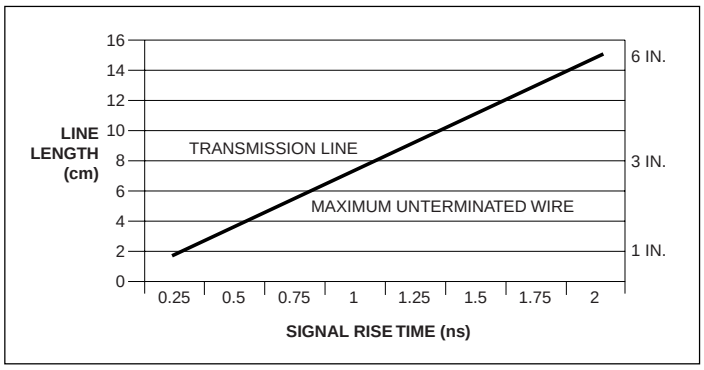

Figure 2. Boundary Between Wire Pairs and Transmission Line

Characteristic Impedance

The permitivity and permeability of the medium in which it travels determines the electromagnetic wave's velocity of propagation. Velocity in free space is $V_0 = 1/\sqrt{(\varepsilon_0\mu_0)} = 300x10^6$ m/s

Permitivity ε, is the ability of a dielectric to store electric potential energy. Permitivity of free space is $\varepsilon_0 = \frac{1}{36\pi} * 10^{-9}$ F/m.

Permeability, μ, is the property of a magnetic substance that determines the degree to which the substance modifies the magnetic flux in the region of a magnetic field that the substance occupies. Permeability of free space is $\mu_0 = 4\pi * 10^{-7}$ H/m.

In free space the electromagnetic wave moves at the speed of light. Electrical signals in conducting wires propagate at a speed dependent on the surrounding medium. Propagation delay is the inverse of propagation velocity

On a PC board the wave moves at the speed of light divided by the square root of the relative dielectric constant. The following table provides some examples.

Propagation Delay of Electromagnic Fields in Various Media

Medium	Delay (ps/in.)	Dielectric Constant
Air (radio waves)	85	1.0
Coax cable (66% velocity)	113	1.8
Coax cable (75% velocity)	129	2.3
FR4 PCB, outer trace	140-180	2.8-4.5
Alumina PCB, inner trace	240-270	8-10

The most important parameter of the transmission line is the characteristic impedance, Z_0, the effective transmission line impedance that the source signal driver sees during the signal's high-speed transition. During that transition the driver sees only Z_0 and does not see the load impedance, which is at the end of the transmission line. $Z_0 = \sqrt{L/C}$

PCB Transmission Line

Today's PCB are made of either Microstrip lines or Striplines.

Microstrip

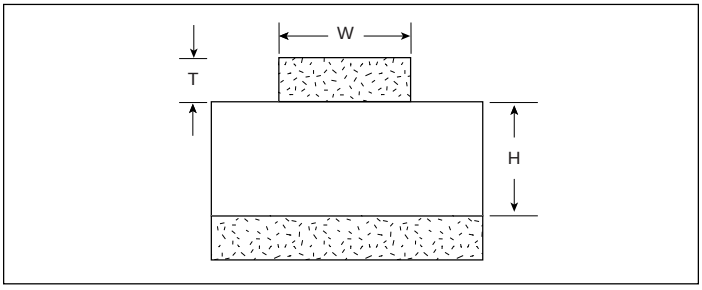

Figure 3. Microstrip

This line consists of two conductors separated by dielectric. The characteristic impedance can be calculated by this formula:

$Z_0 = (87/\sqrt{\varepsilon_R + 1.41})\ln(5.98H/(0.8W+T))$.

This is an n approximation formula that is good enough for most situations. For more precise formulas, please check the references at the end of this note.

Stripline

This line consists of a strip of conductor in the middle of two conducting planes.

The equation: $Z_0 = (60/\sqrt{\varepsilon_R})\ln(4B/0.67\pi W(0.8 + (TW)))$.

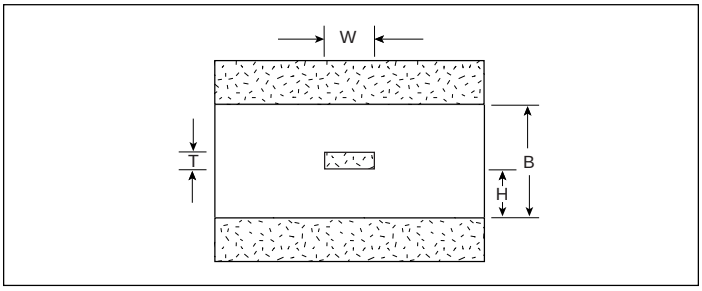

Figure 4. Stripline

The following are some trace geometry examples:

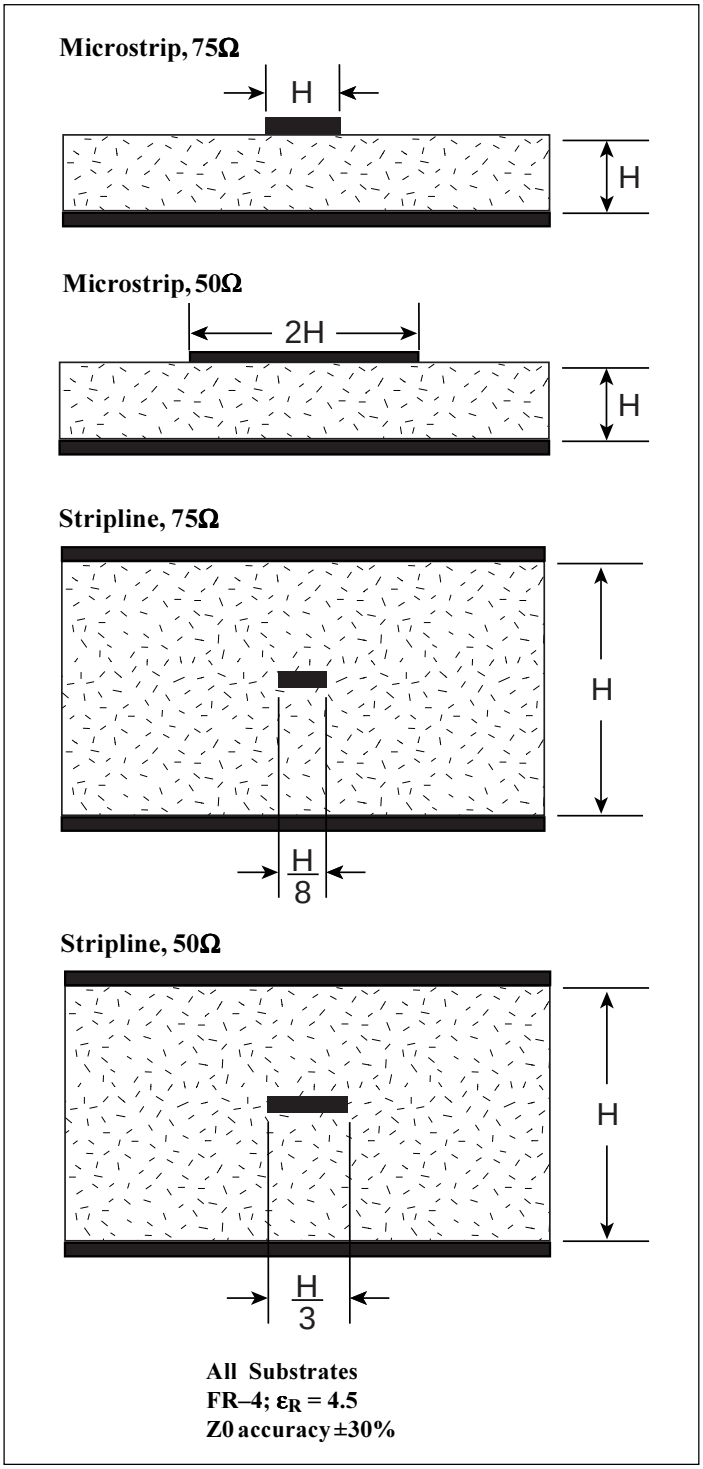

Figure 5. Cross Sections of Approximate Trace Geometries Need to Produce 50- and 75-Ohm Transmission Lines

Multiple Loads on a Transmission Line

The above formulas apply if the trace have a single load . But with two or more loads use the following formulas:

$$Z_0' = Z_0 + \sqrt{1 + C_l/C_O}$$

$$T'_{PD} = t_{PD}\sqrt{1 + C_l/C_O}$$

Cl is the added load capacitance per unit length.

Transmission Line Analysis

When using transmission line analysis it is important to remember that if the line is not matched, then there will be reflections that will introduce ringing. Ringing will take away from the system margin. if the load impedance Z_l does not match Z_0, then the signal energy that the load does not absorb reflects back toward the source. When the reflection reaches the source, if the source impedance does not match Z_0, there is a reflection from the source back to the load. The reflections continue until the load, the source, and losses along the transmission line fully absorb the source energy.

The reflection formula can be derived by the following:

$$V_l = V_{incident} + V_{reflected}$$
$$I_l = I_{incident} + I_{reflected} \cdot$$
$$\text{Reflection factor } \rho = Z_l - Z_0 / Z_l + Z_0$$

Note: If $Z_l = Z_0$ then the reflection is zero , the optimum operating situation.

If Z_l = Infiniti, then $\rho = 1 - z0/zl / (1 + z0/zl) = 1$

$\rho = 1$ or the whole incident wave will be reflected back if your input is 5 volts. You will then see 9 to 8 volts at the receiver, (see Fig.6)

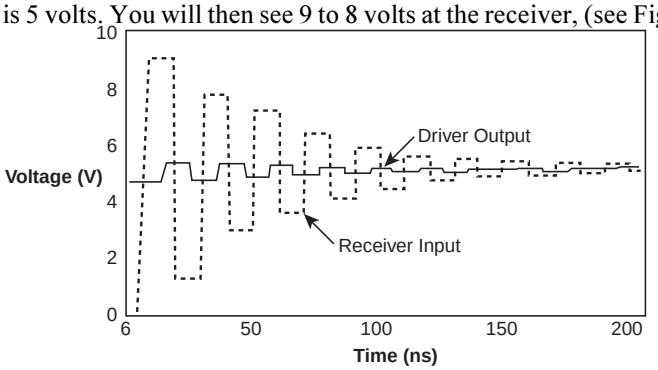

Figure 6. Reflections Due to Mismatched Transmission Line

Termination Techniques

It is very important to properly terminate the transmission line. In this section we will discuss the termination techniques available to ensure that the high-speed system board will work according to plan and with considerable noise margin. The following are several termination techniques: series, parallel, Thevenin, AC, and diode-based. Advantages and disadvantages for each will be discussed.

Series Termination

Series termination is source-end matching. Easy to apply, it is a series resistor that is inserted as close to the source as possible, see following figure:

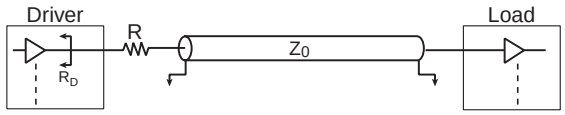

Figure 7. Series Terminator

The sum of the output impedance of the driver and the series resistor should be equal to Z0 which is the characteristic impedance of the board trace. With this termination we still have a mismatch at the receiver's end. The receiver typically has very high input impedance. A mismatch will cause a reflection of the same voltage magnitude as the incident wave. The receiving device sees the sum of the incident and reflected voltages (full voltage) and the added signal propagates to the driving end. Since the line is matched at the driving end, no further reflections occur.

The series termination has the following disadvantages:

1. Difficult to tune the value of the series resistor so that you have a precisely matched line. The output impedance of the driver changes depending on the output and the load.
2. The driving end of the transmission line does not see the full voltage until the round trip. This may cause problems in multi-drop systems.

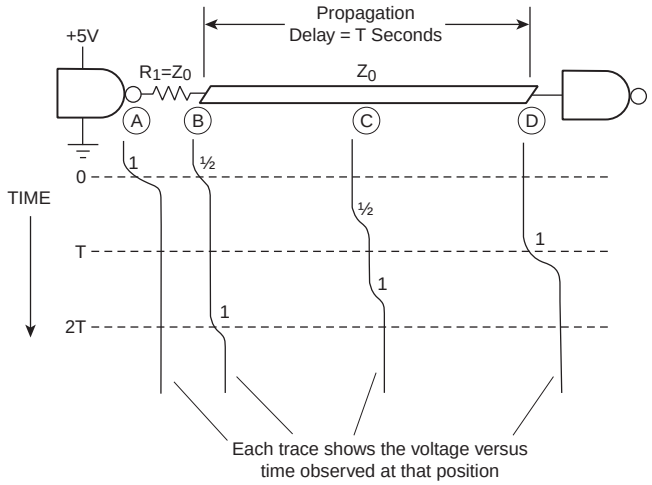

Figure 8.

3. To cut down the noise margin, the designer must accommodate for the delay in the setup time.
4. The rise time of the circuit will be slowed by the receiver's capacitive load. Therefore you have to add a delay of the Z_0C time constant.

The series termination has the following advantages:

1. Series termination adds only one resistor to the circuit.
2. This type of termination does not add any DC load.
3. Power comsuption is the lowest. No extra impedance is added to ground.

Parallel Termination

This is also called end termination. For this termination the designer must insert a resistor equal to the Z_0 of the trace. This resistor is located close to the receiver and it is connected to ground or V_{CC}.

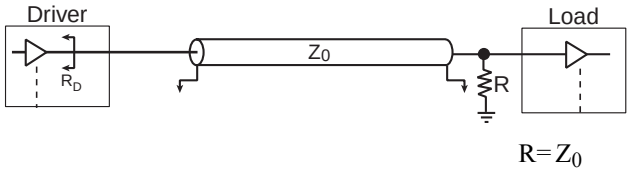

Figure 9. Example of Parallel Termination

The driving waveform propagates fully all the way down the transmission line. Since the transmission line is matched, there will be no reflections back and forth

Advantages

1. It is an easy and simple single resistor termination.
2. The signal's rise time is delayed by the $Z_0C/2$ time constant as compared with a Z_0C time constant of a series termination.

Disadvantages

1. More power is dissipated through the termination resistor.
2. The driver needs to supply additional DC current to the termination resistor. If Z_0 = 50ohms, the DC current can be very high. I = 5/50 = 100mA; large for CMOS circuitry.
3. This termination to ground will cause the falling edge to be faster then the rising edge. This might change the duty cycle.

Thevenin Termination

This is also called dual termination. Two resistors R1 and R2 are connected to the receiver as shown in the following figure:

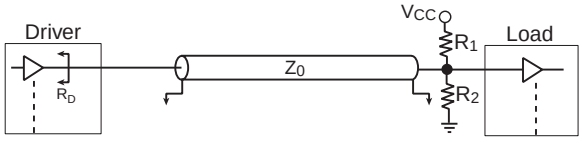

Figure 10. Example of Thevenin Termination

$$Z0 = \frac{R_1 R_2}{R_1 + R_2}.$$

We must not exceed IOH and IOL max. This circuit is not recommended in TTL or CMOS circuits owing to the large currents required in the HI state.

Other terminations that are not recommended

AC Termination

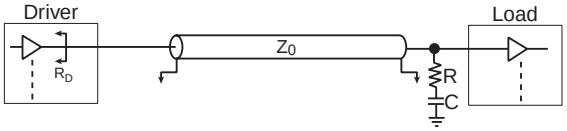

Figure 11. Example of AC Termination

Diode Termination

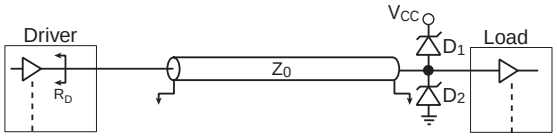

Figure 12. Example of Schottky Diode Termination

Decoupling Capacitors

Every printed circuit board needs large bypass capacitors to balance the inductance of the power supply wiring. Every capacitor has some lead inductance that increases as the frequency goes higher. That is why it is very important to place the capacitors as close to the V_{CC} pin on the chip as possible.

To reduce the series lead inductance effect, avoid the following:

1. long traces larger then 0.01 inch between the capacitor pad and the via.
2. use of capacitors other than surface mount.
3. skinny via holes less than an 0.035-inch diameter.

Pericom's clock product lines uses high-precision integrated analog PLLs that are sensitive to noise on the supply and ground pins which can dramatically increase the skew and output jitter.

For maximum protection connect a 0.1µF and a 2.2 nF capacitor to every digital supply pin. Also use three 4.7µFs, one 220nF, and one 2.2µF capacitor on the analog supply pin. Connect the other side to the analog ground pin. If you are limited on space a 0.1µF capacitor on every supply line will work.

Place a 10µF cap from the main Power Island to the power plane supplied to the clock chip.

Use high quality, low ESR, ceramic surface-mount capacitors.

Stacking

At low speeds currents follow the least resistant path, but at high speeds the current follows the least inductance path. The lowest inductance return path lies directly under the signal conductor, thereby minimizing the total loops between the outgoing and returning paths. That is why, if possible, it is important to separate the signal layers by ground planes. Also, do not cut part of the ground plane to be used for a signal's path. That is totally unacceptable, because it will increase crosstalk considerably. Besides, it does not provide a clean return to those signals. Also use lower trace impedance since it will lower undershoot and overshoot. Best to use FR-4 material for board fabrication.

Use 4- layer stack-up arrangement. Make sure you have a signal layer followed by the ground layer, then the power layer, and finally the second signal layer. See Figure 13. shown below:

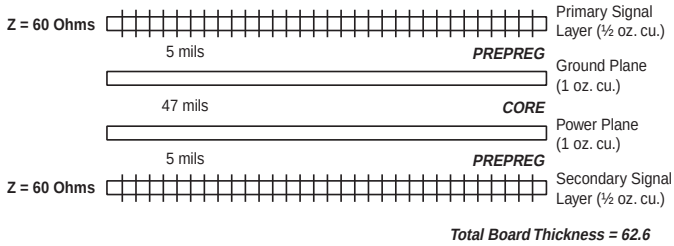

Figure 13. Four-Layer Board Stack-up

Clock routing and spacing

To minimize crosstalk on the clock signals, we must use a minimum of 0.014-inch spacing between the clock traces and others. If you have to use serpentine to match trace lengths on similar chips, make sure that you have at least 0.018-inch spacing for those serpentines. Serpentines are not recommended for clock signals.

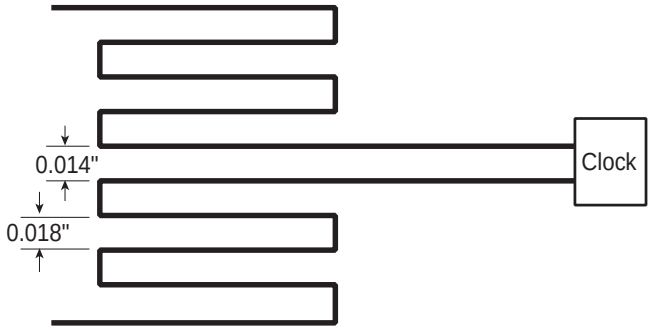

Figure 14. Clock Trace Spacing Guidelines

As we discussed in an earlier section, you need to terminate the transmission line. Use a series resistor closest to the source to drive the transmission line. Most of Pericom clock products have approximately an 25-ohm output impedance, so, if the impedance or the transmission line is 65 ohms, use a series resistor of 40 ohms . Clock traces should be between 1- and 10-inches long. To verify that the clock delay, undershoot, overshoot, and skew are within the system's AC parameters, it is important that the designer perform prelayout and post layout signal integrity simulation on the clock lines. Pericom Provides IBIS models for the entire clock product line.

If you are forced to make a tee perform the following:

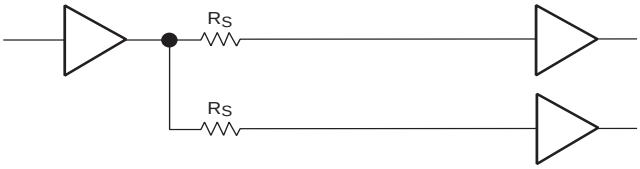

Figure 15. Series Termination, Multiple Loads

General Guidelines

1. Limit your trace lengths. Longer traces display more resistance and induction and introduce more delays. It also limits the bandwidth which varies inversely with the square of trace length.
2. Use higher impedance traces. Raising the impedance will also increase the bandwidth. Use 65-ohm impedance.
3. Do not use any clock signal loops. Keep clock lines straight when possible.
4. For related clock signals that have skew specifications, match the clock trace lengths. For example, PCI expansion slots.
5. Do not route any signals in the ground and V_{CC} planes.
6. Do not route signals close to the edge of the PCB board.
7. Make sure there is a solid ground plane beneath the clock chip.
8. The power plane should face the return ground plane. No signals should be routed between.
9. Route clock signals on the top layer and make sure that there are no vias. Vias change the impedance and introduce more skew and reflections.
10. Do not use any connectors on clock traces.
11. Use wide traces for power and ground.
12. Keep high-speed switching busses and logic away from the clock chip.
13. Place the clock chip in the center of all chips, so that clock signal traces are kept to a minimum.

References

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   Prentice Hall, 1993.
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3. C. Pace "Terminate Bus lines to Avoid Overshoot and Ringing", EDN, pp227-234 Sept -1987
4. J.Sutherland "As Edge Speeds Increase, Wires Become Transmission Lines", EDN, pp75-85 Oct - 1999
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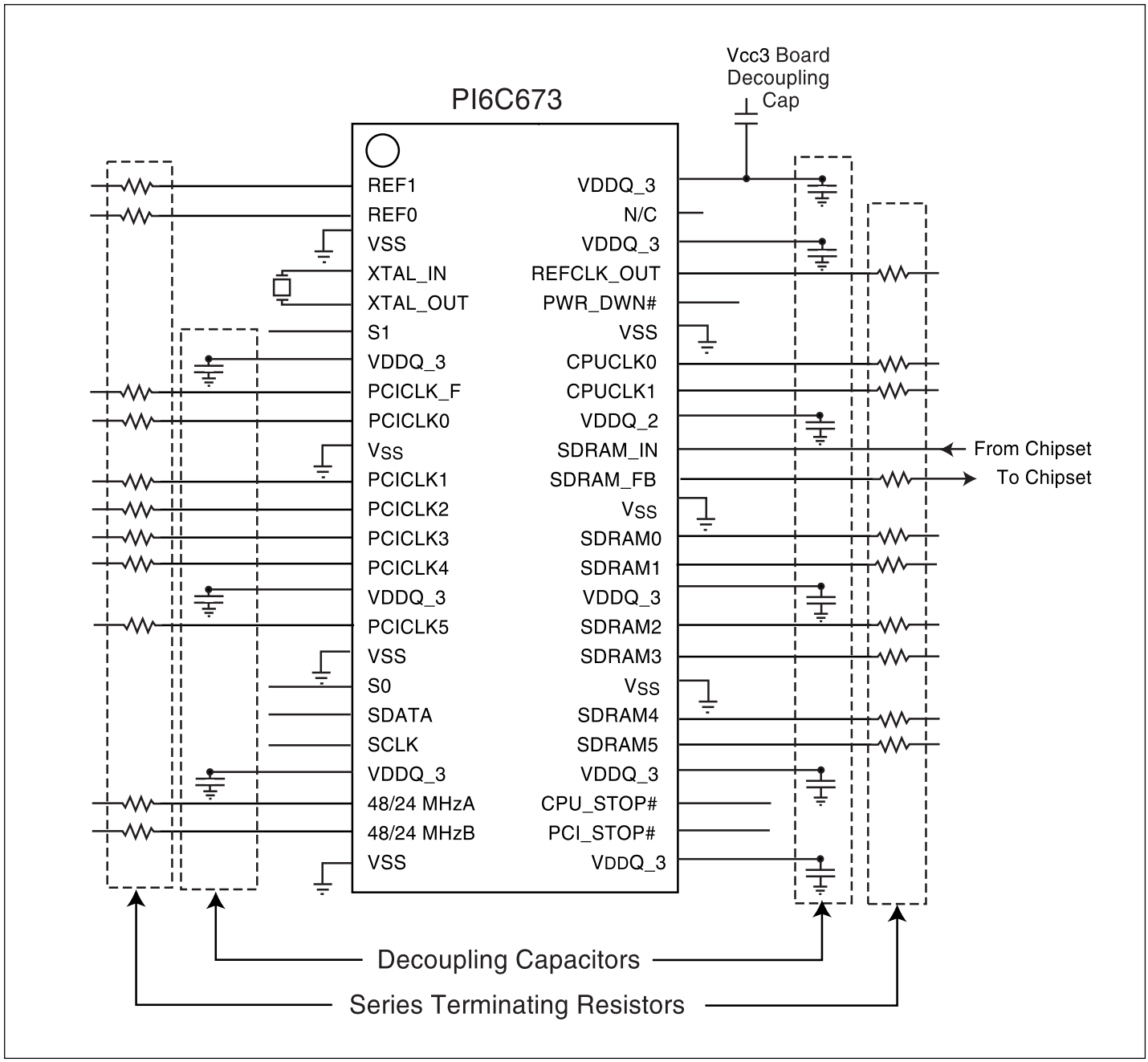

Figure 16. Schematic Drawing

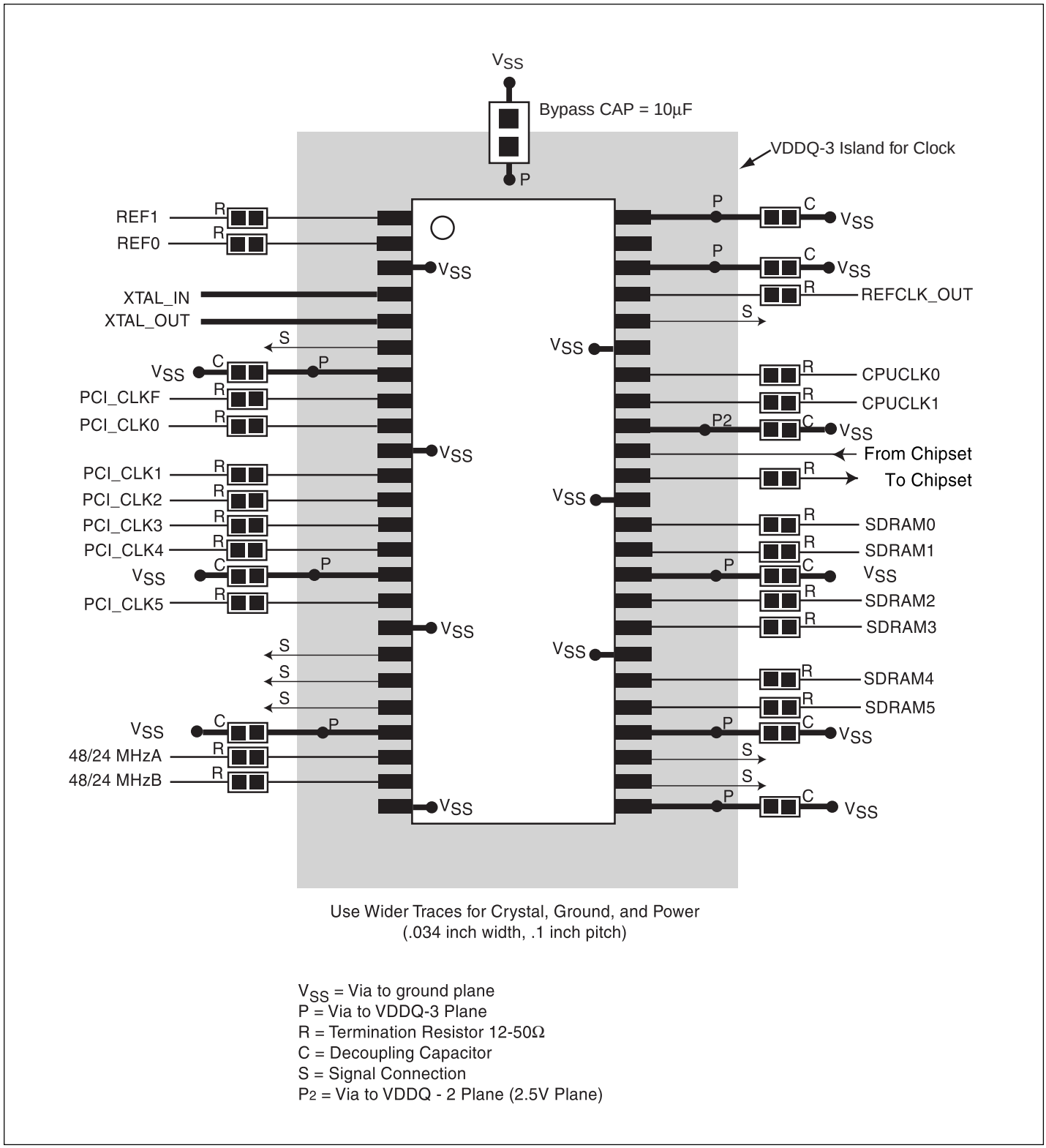

Figure 17. PI6C673 Layout